1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,X425

08/06/2014 PROTO1A

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00330	1	SCHEM,MLB,X305	SCH	CRITICAL	
820-00138	1	PCBF,MLB,X305	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Wed Aug 6 13:00:04 2014

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 118
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00039	COMMON PARTS,MLB,X425	X425_COMMON
985-00043	DEV,MLB,X425	X425_DEVEL:ENG
639-00534	PCBA,MLB,CTO,16G-HYN,X425	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1866
639-00535	PCBA,MLB,CTO,16G-MIC,X425	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1866

X425 BOM Groups

BOM GROUP	BOM OPTIONS
X425_COMMON	ALTERNATE,COMMON,X425_COMMON1,X425_COMMON2,X425_PROGPARTS
X425_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CPUPEG:X8X8,S2_PWR:S0,SMC_SUSACK:YES
X425_COMMON2	EDP:YES,XDP,SSD_PWR_EN:GPIO,CAM_WAKE:NO,SAMCONN,APCLKRQ:ISOL,DDRREG_PGD:N,CRW_SPRT,WLAN_SW:SIL
X425_PVT	BKLT:PROD,SENSOR_NONPROD:N
X425_PROGPARTS	SMC_PROG:BASE,BOOTROM_PROG:PROTO1A,TBTROM:PROG
X425_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,X249:BOOST
X425_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
X425_DEVEL:PVT	XDP_DEBUG
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00057	1	CRW,SR1ZW,PRQ,C0,2.2,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S00058	1	CRW,SR1ZX,PRQ,C0,2.5,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S00059	1	CRW,SR1ZY,PRQ,C0,2.8,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QENV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0802	16	IC,SDRAM,2SNM,512MX8,DDR3L-1866,78B FBGA		CRITICAL	HYNIX_1866_S
333S0719	16	IC,SDRAM,4GBIT,DDR3-1866,VB0A,78B,FBGA		CRITICAL	MICRON_1866_S
333S0802	32	IC,SDRAM,2SNM,512MX8,DDR3L-1866,78B FBGA		CRITICAL	HYNIX_1866
333S0719	32	IC,SDRAM,4GBIT,DDR3-1866,VB0A,78B,FBGA		CRITICAL	MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1866_S	HYNIX_1866_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1866_S	MICRON_1866_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:HYNIX_1866	HYNIX_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1866	MICRON_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00039	1	COMMON PARTS,MLB,X425	BASE	CRITICAL	BASE_BOM
985-00043	1	DEV,MLB,X425	DEVEL	CRITICAL	DEVEL_BOM

SYNC_MASTER=CLEAN_X305 SYNC_DATE=05/30/2014

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S00133	1	T29,FALCON RIDGE(VXXXX)PROTO 1A,X425	U2890	CRITICAL	TBTROM:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BLANK
341S00125	1	IC,SMC-B1,EXT (V2.24A31) PROTO 1A,X425	U5000	CRITICAL	SMC_PROG:BASE

EFI ROM

335S00007	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:WIN
335S00006	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:MAC
341S00131	1	IC,EFI ROM (VXXXX) PROTO 1A,X425	U6100	CRITICAL	BOOTROM_PROG:PROTO1A

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S00008		ALL	Panasonic alt to TDK
376S1217	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
128S0371	128S0376		ALL	Kemet alt to Sanyo
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX
311S0649	311S0541		ALL	ON alt to Toshiba
376S00014	376S0761		ALL	Toshiba alt to Vishay
740S00003	740S0135		ALL	AEM alt to Tyco
377S0155	377S00011		ALL	On Semi alt to Infineon
377S0184	377S00011		ALL	Infineon alt to Infineon

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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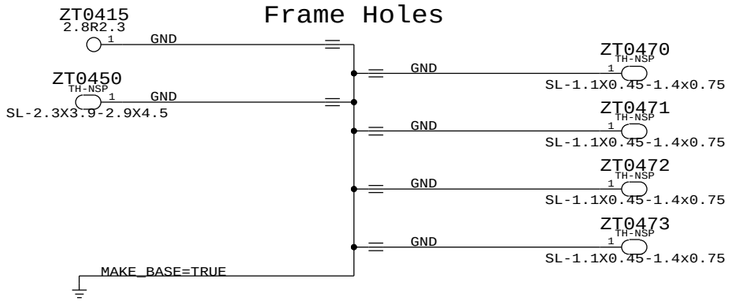
Frame Holes



X425 THERMAL MODULE STANDOFF

860-00173

SH0427
5.0OD1.85ID-2.35H-SM

SH0426
5.0OD1.85ID-2.35H-SM

SH0429
5.0OD1.85ID-2.35H-SM

SH0428
5.0OD1.85ID-2.35H-SM

860-00184

OMIT_TABLE
SH0425
STDOFF-4.5OD1.8H-SM

OMIT_TABLE
SH0423
STDOFF-4.5OD1.8H-SM

860-00167

SH0424
4.5OD1.9H-SM-X304

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-00184	2	STANDOFF,THERMAL/FAN,W/O MYLAR,X305	SH0423,SH0425	CRITICAL	

817-00335
SH0446
5.0OD2.9ID-2.38H

817-00336
SH0445
5.0OD2.9ID-2.38H-FD2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	

806-9391
SH0450
SM
SHLD-MLB-USB-J45

806-00452
SH0451
SM
SHLD-FENCE-MLB-T29-X305

APN 806-2247
BR0401
MLB-MTG-BRKT-J5

X425 POGO PINS

SH0431
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM

SH0432
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM

SH0433
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM

SH0437
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM

SH0434
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM

SH0435
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM

SMT GND TEST PONTS

ZT0490
2.1SM2.0MM-CIR
SMT-PAD-NSP

ZT0491
2.1SM2.0MM-CIR
SMT-PAD-NSP

ZT0492
2.1SM2.0MM-CIR
SMT-PAD-NSP

RIO FLEX BRACKET BOSS (860-00166)

SH0480
3.5OD1.85ID-2.0H

SH0481
3.5OD1.85ID-2.0H

X425 StAND OFF

860-1448

SH0440
2.9OD1.2ID-1.35H-SM

SH0443
2.9OD1.2ID-1.35H-SM

SH0460
2.9OD1.2ID-1.35H-SM

SH0462
2.9OD1.2ID-1.35H-SM

SH0466
2.9OD1.2ID-1.35H-SM

SH0470
2.9OD1.2ID-1.35H-SM

SH0472
2.9OD1.2ID-1.35H-SM

SH0474
2.9OD1.2ID-1.35H-SM

SH0441
2.9OD1.2ID-1.35H-SM

SH0444
2.9OD1.2ID-1.35H-SM

SH0461
2.9OD1.2ID-1.35H-SM

SH0465
2.9OD1.2ID-1.35H-SM

SH0467
2.9OD1.2ID-1.35H-SM

SH0471
2.9OD1.2ID-1.35H-SM

SH0473
2.9OD1.2ID-1.35H-SM

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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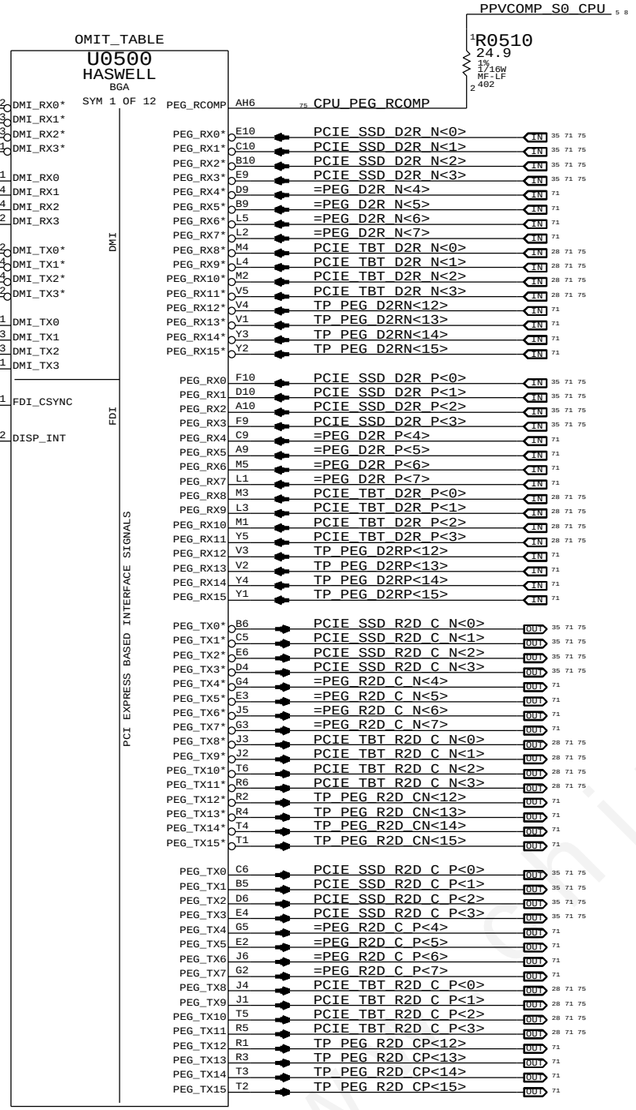

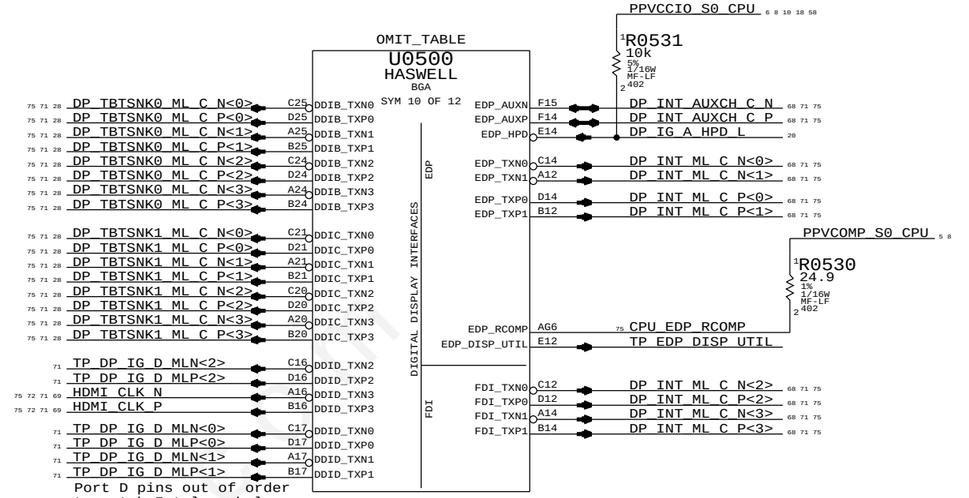

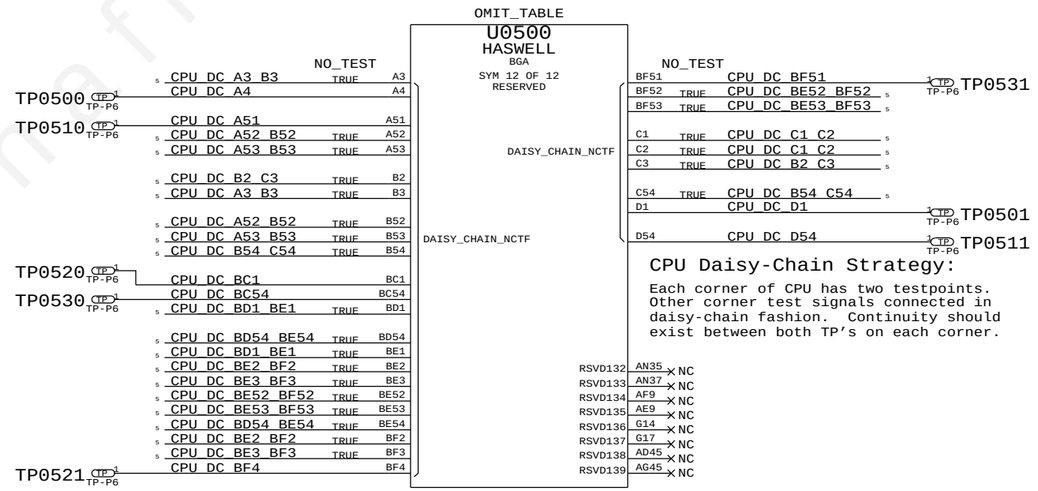

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

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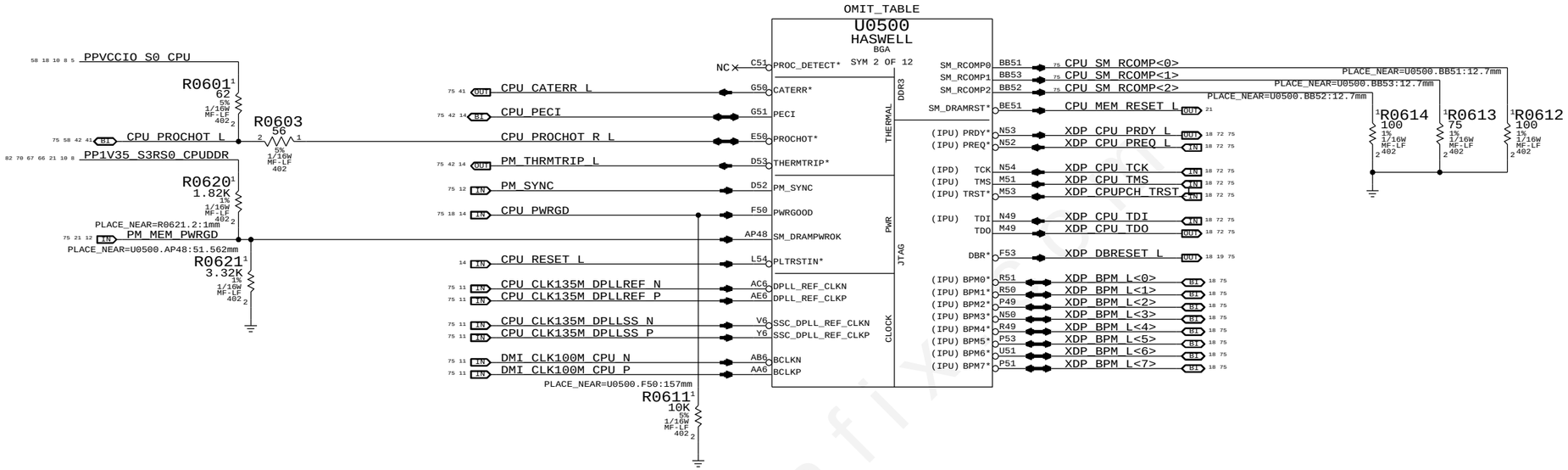
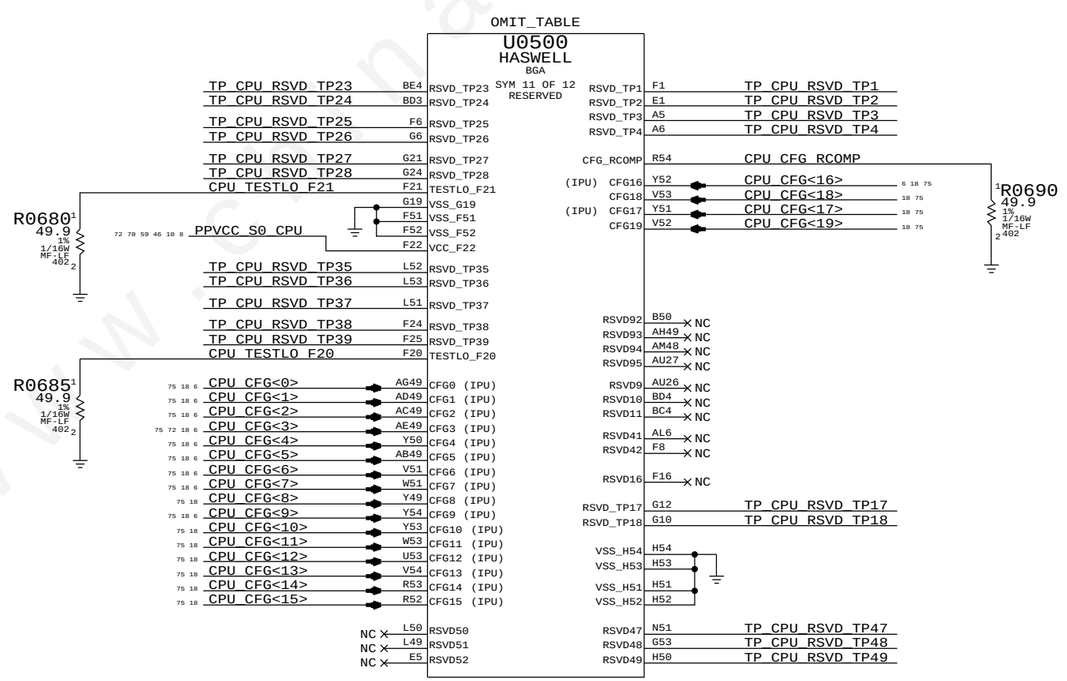
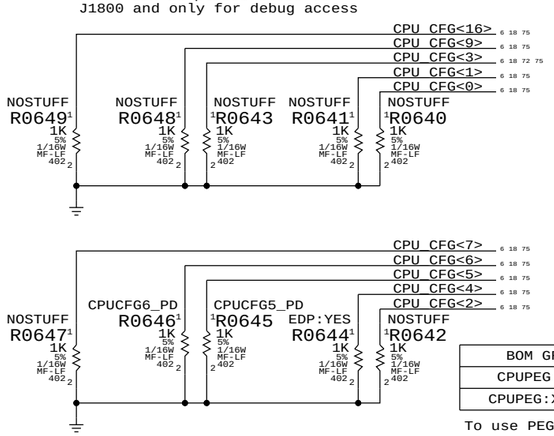




CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Clock/Misc/JTAG/CFG

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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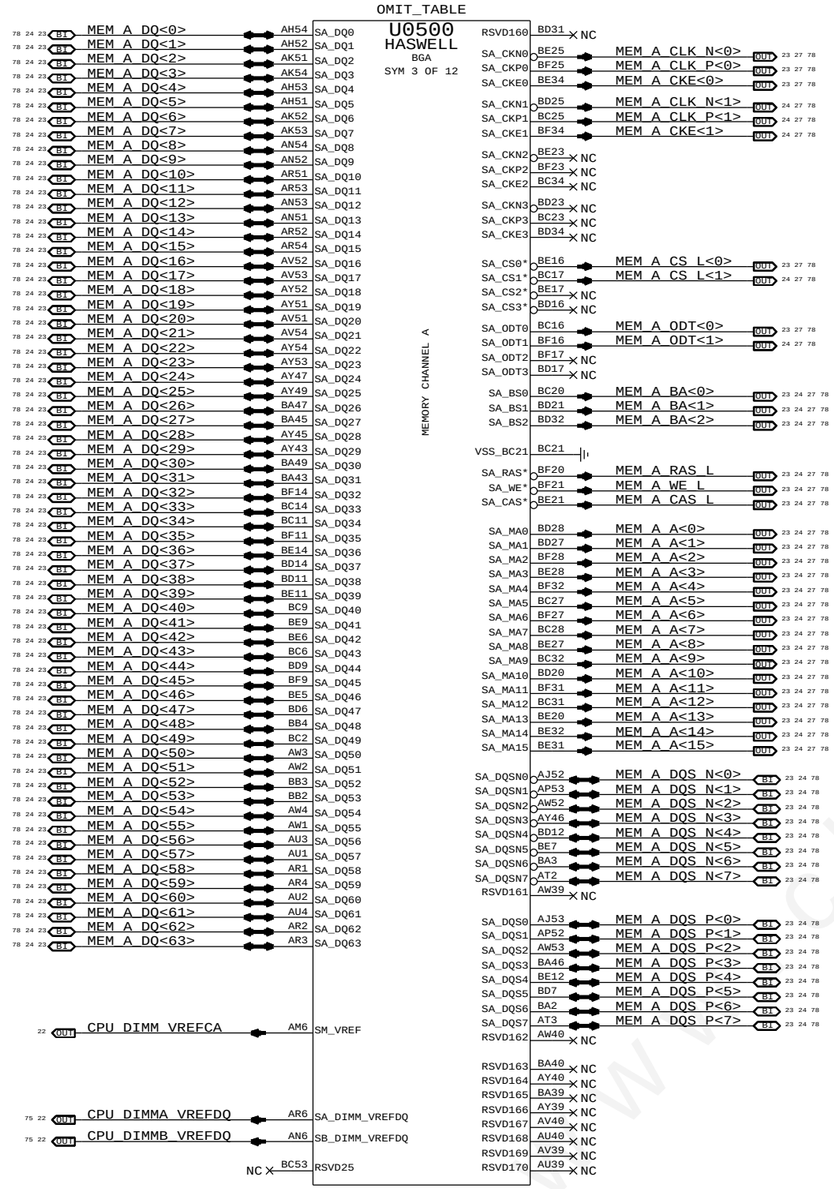

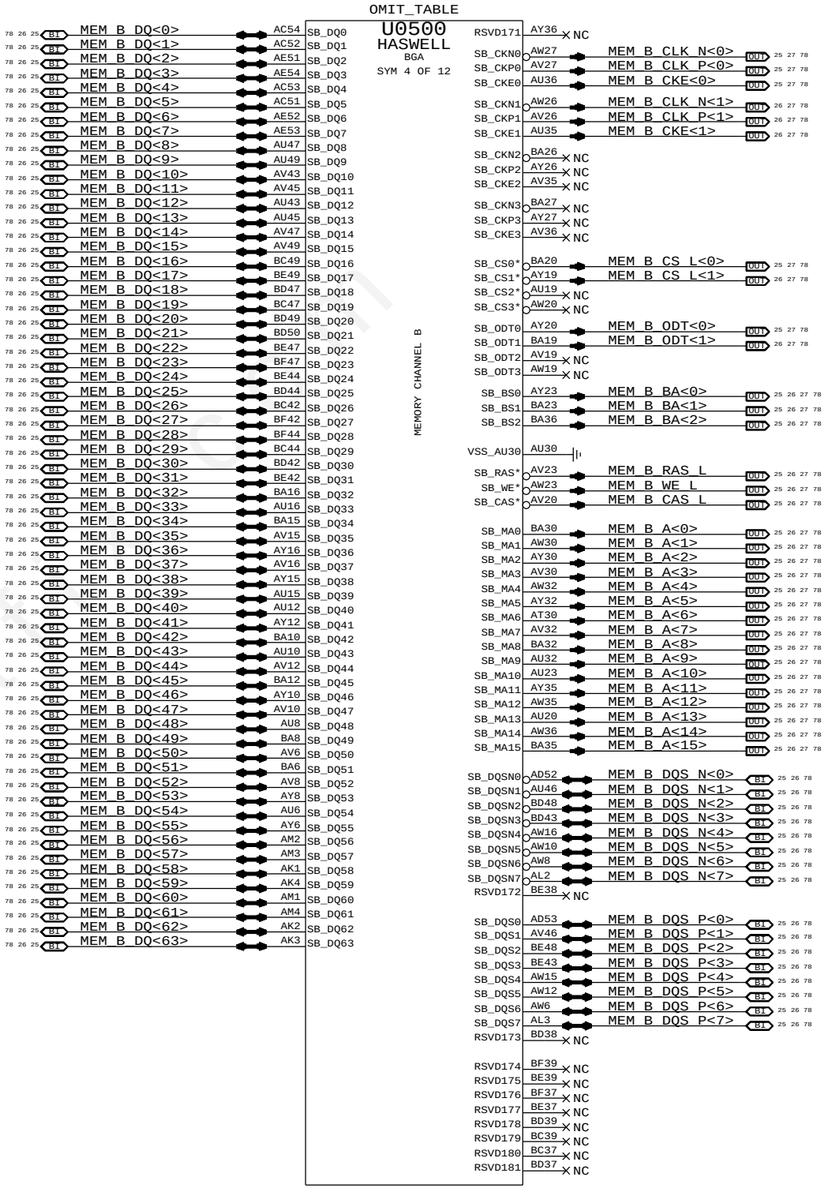

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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	PAGE 7 OF 118
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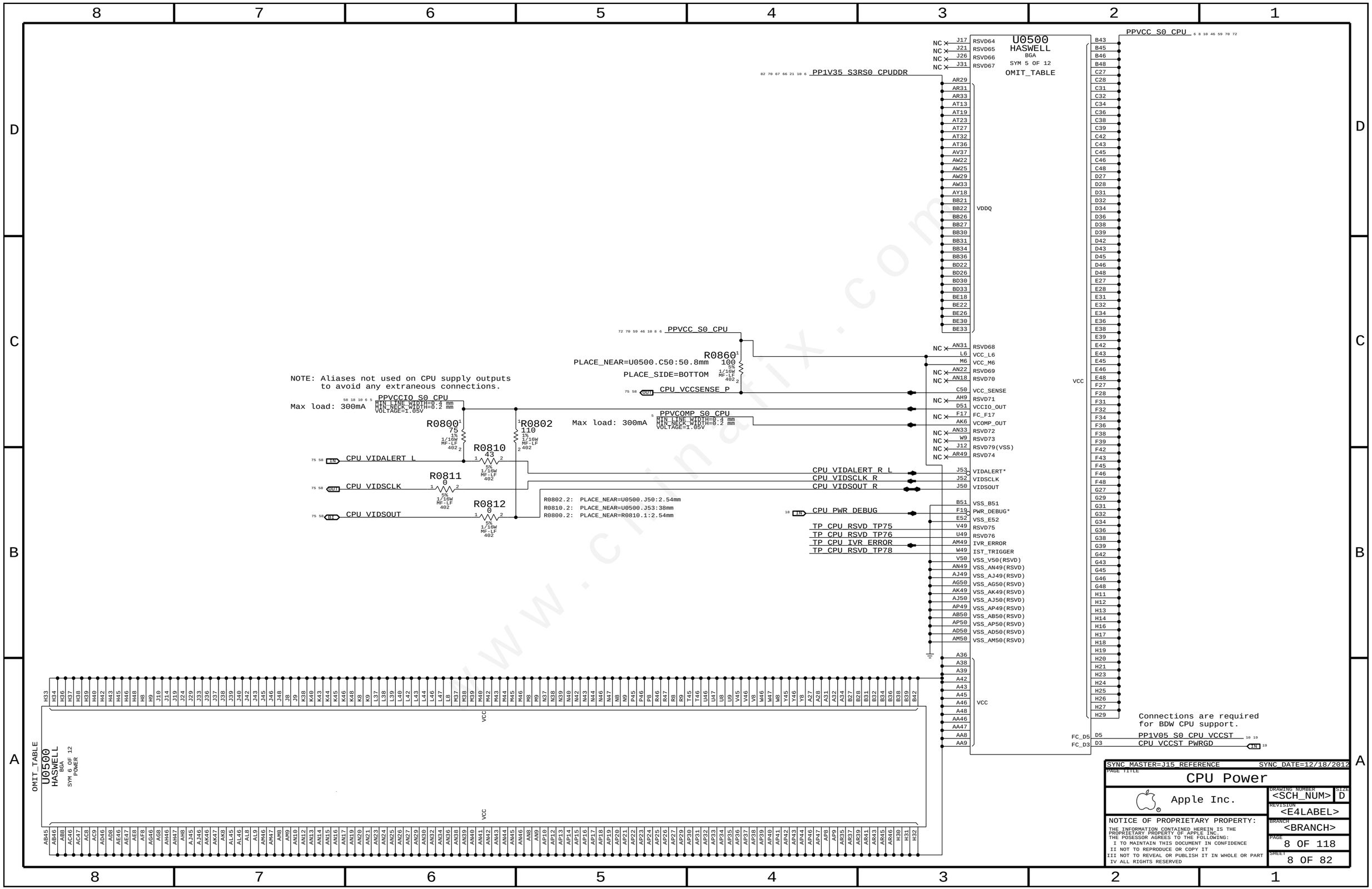
U0500
HASWELL
BGA
SYM 5 OF 12
OMIT_TABLE
PP1V35_S3RS0_CPUDDR
PPVCC_S0_CPU
VDDQ
VCC
NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.
PPVCCIO_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
R0800 75 1% 1/10W MF-LF 402
R0802 110 1% 1/16W MF-LF 402
R0810 43 5% 1/16W MF-LF 402
R0811 0 5% 1/16W MF-LF 402
R0812 0 5% 1/16W MF-LF 402
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
R0860 100 1% 1/10W MF-LF 402
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
CPU_VCCSENSE_P
PPVCOMP_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_PWR_DEBUG
TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_IVR_ERROR
TP_CPU_RSVD_TP78
Connections are required
for BDW CPU support.
PP1V05_S0_CPU_VCCST
CPU_VCCST_PWRGD
SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012
PAGE TITLE
CPU Power
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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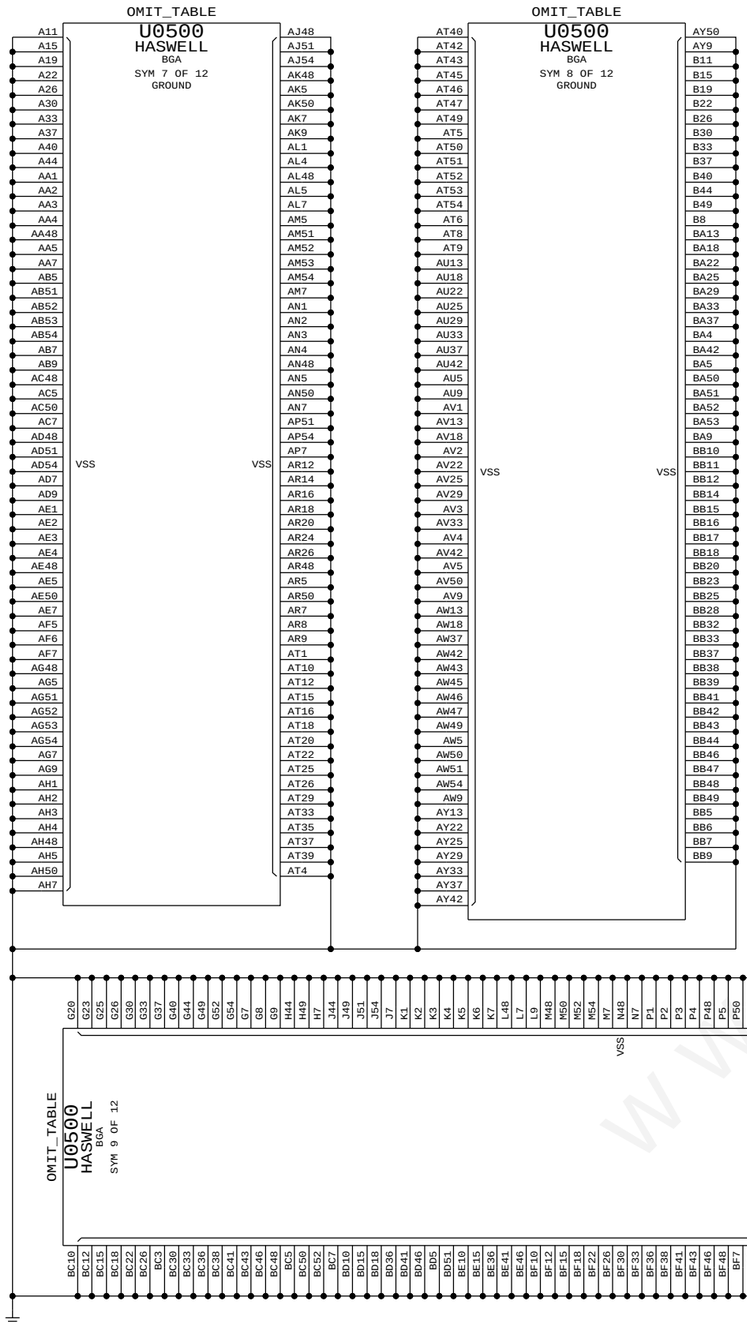

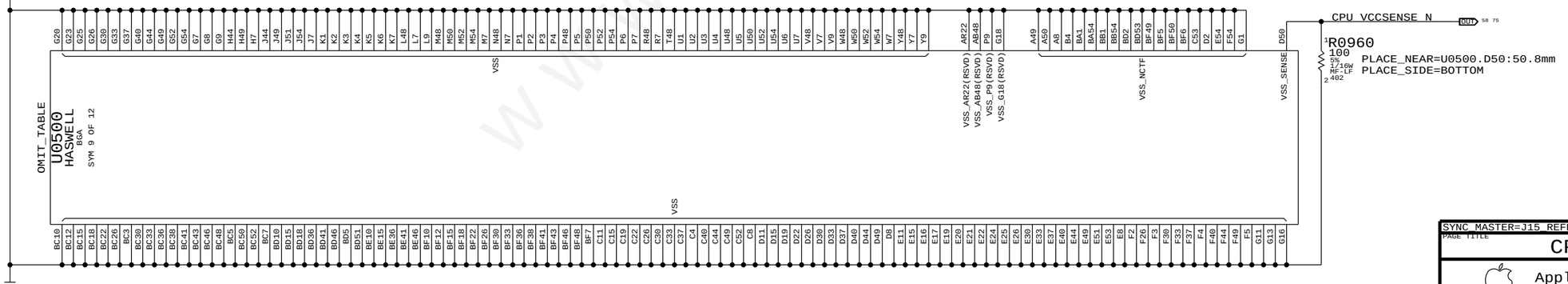

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

CPU Ground

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1001 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1002 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

C1020 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1021 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1022 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1023 20UF 20% 4V X5R-CERM 0402-2

CAPs for Acoustic control (C109A-C102D)

C109A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1025 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1026 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1027 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1028 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1029 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1030 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1031 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1032 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1033 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1034 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1035 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1036 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1037 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1038 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1039 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1040 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1041 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1042 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1043 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1044 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1045 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1047 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1048 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1049 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1050 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1051 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1052 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1053 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1054 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1055 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1056 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1057 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1058 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1059 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1060 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1061 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1062 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1063 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1064 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1065 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1066 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1067 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1068-C1076:

NO STUFF NO STUFF
CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1077 210UF 20% 2.5V POLY-TANT CASE-B2S

CAPs for Acoustic control (C102E-C103F)

C102E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

PP1V35_S3RS0_CPUDDR

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S 0402
C1091 10UF 20% 4V X6S 0402
C1092 10UF 20% 4V X6S 0402
C1093 10UF 20% 4V X6S 0402
C1094 10UF 20% 4V X6S 0402
C1095 10UF 20% 4V X6S 0402
C1096 10UF 20% 4V X6S 0402
C1097 10UF 20% 4V X6S 0402

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2V POLY-TANT D1ST-ECGLT-COMBO
CRITICAL C1099 330UF-6MOHM 20% 2V POLY-TANT D1ST-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

PPVCCIO_S0_CPU

C1079 0.01UF 10% 10V X7R-CERM 0402

CPU VCCST Decoupling

Intel recommendation: 1x 0.1uF 0402, 1x 4.7uF 0805
Apple Implementation: 1x 0.1uF 0201, 1x 4.7uF 0402

PP1V05_S0

BDW_SPRT R1080 0 5% 1/10W MF-LF 603

PP1V05_S0_CPU_VCCST
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PLACE_NEAR=U0500.D5:25.4mm
PLACE_NEAR=U0500.D5:12.7mm

BDW_SPRT C108A 0.1UF 10% 6.3V CERM-X5R 0201
BDW_SPRT C108B 4.7UF 20% 6.3V X5R 402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
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BRANCH: <BRANCH>
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OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(1 OF 11)

RTC
SATA
AZALIA
JTAG

SYSCLK_CLK32K_RTC — RTCX1 (B5); RTCX2 (B4) NC
PCH_SRTCRST_L — SRTCRST* (B9)
PCH_INTRUDER_L — INTRUDER* (A8)
PCH_INTVRMEN_L — INTVRMEN (G10)
RTC_RESET_L — RTCRST* (D9)

HDA_BIT_CLK — R1110 33 — HDA_BIT_CLK_R — HDA_BCLK (B25)
HDA_SYNC — R1111 33 — HDA_SYNC_R — HDA_SYNC (IPD-boot) (A22)
PCH_SPKR — SPKR (IPD-PLTRST#) (AL10)
HDA_RST_L — R1112 33 — HDA_RST_R_L — HDA_RST* (C24)
HDA_SDIN0 — HDA_SDI0 (IPD) (L22)
NC_HDA_SDIN1 — HDA_SDI1 (IPD) (K22)
NC_HDA_SDIN2 — HDA_SDI2 (IPD) (G22)
NC_HDA_SDIN3 — HDA_SDI3 (IPD) (F22)
HDA_SDOUT — R1113 33 — HDA_SDOUT_R — HDA_SDO (IPD-boot) (A24)
DP_TBT_SEL — DOCKEN*/GPIO33 (IPD-DOCKENM#2) (B17)
ENET_MEDIA_SENSE_RDIV — HDA_DOCK_RST*/GPIO13 (C22)

XDP_PCH_TCK — JTAG_TCK (IPD) (AB3)
XDP_PCH_TMS — JTAG_TMS (IPU) (AD1)
XDP_PCH_TDI — JTAG_TDI (IPU) (AE2)
XDP_PCH_TDO — JTAG_TDO (AD3)
NC — TP25 (F8)
NC — TP22 (C26)
NC — TP20 (AB6)

SATA_RXN0 BC8 NC_SATA_A_D2RN
SATA_RXP0 BE8 NC_SATA_A_D2RP
SATA_TXN0 AW8 NC_SATA_A_R2D_CN
SATA_TXP0 AY8 NC_SATA_A_R2D_CP
SATA_RXN1 BC10 NC_SATA_B_D2RN
SATA_RXP1 BE10 NC_SATA_B_D2RP
SATA_TXN1 AV10 NC_SATA_B_R2D_CN
SATA_TXP1 AW10 NC_SATA_B_R2D_CP
SATA_RXN2 BB9 NC_SATA_ODD_D2RN
SATA_RXP2 BD9 NC_SATA_ODD_D2RP
SATA_TXN2 AY13 NC_SATA_ODD_R2D_CN
SATA_TXP2 AW13 NC_SATA_ODD_R2D_CP
SATA_RXN3 BC12 NC_SATA_D_D2RN
SATA_RXP3 BE12 NC_SATA_D_D2RP
SATA_TXN3 AR13 NC_SATA_D_R2D_CN
SATA_TXP3 AT13 NC_SATA_D_R2D_CP
SATA_RXN4/PERN1 BD13 TP_PCIE_ENET_D2RN
SATA_RXP4/PERP1 BB13 TP_PCIE_ENET_D2RP
SATA_TXN4/PETN1 AV15 TP_PCIE_ENET_R2D_CN
SATA_TXP4/PETP1 AW15 TP_PCIE_ENET_R2D_CP
SATA_RXN5/PERN2 BC14 NC_SATA_F_D2RN
SATA_RXP5/PERP2 BE14 NC_SATA_F_D2RP
SATA_TXN5/PETN2 AP15 NC_SATA_F_R2D_CN
SATA_TXP5/PETP2 AR15 NC_SATA_F_R2D_CP
SATA_RCOMP AY5 — PCH_SATA_RCOMP
SATALED* AP3 — PCH_SATALED_L
SATA0GP/GPIO21 AT1 — XDP_DC0_DP_AUXCH_ISOL_L
SATA1GP/GPIO19 (IPU-PLTRST#) AU2 — XDP_DC1_SATARDRVR_EN
SATA_IREF BD4
TP9 BA2 NC
TP8 BB2 NC

SATA Port assignments:

Primary HDD/SSD (SATA only)

Secondary HDD/SSD (SATA only)

Reserved: ODD

Unused

PCIe:
Reserved: Ethernet
(if not combo w/SD Card)

Unused

PP1V5_S0 — R1130 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.AY5:2.54mm

NOTE: ENET pair only used if SD Card Reader is USB3.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(2 OF 11)

CLOCKS

PCIE_CLK100M_SSD_N — CLKOUT_PCIE_N0 (Y43)
PCIE_CLK100M_SSD_P — CLKOUT_PCIE_P0 (Y45)
SSD_CLKREQ_L — PCIECLKRQ0*/GPIO73 (AB1)
NC_PCIE_CLK100M_ENETSDN — CLKOUT_PCIE_N1 (AA44)
NC_PCIE_CLK100M_ENETSDP — CLKOUT_PCIE_P1 (AA42)
XDP_DD2_ENETSD_CLKREQ_L — PCIECLKRQ1*/GPIO18 (AF1)
PCIE_CLK100M_AP_N — CLKOUT_PCIE_N2 (AB43)
PCIE_CLK100M_AP_P — CLKOUT_PCIE_P2 (AB45)
XDP_DD3_AP_CLKREQ_L — PCIECLKRQ2*/GPIO20/SMI* (AF3)
PCIE_CLK100M_CAMERA_N — CLKOUT_PCIE_N3 (AD43)
PCIE_CLK100M_CAMERA_P — CLKOUT_PCIE_P3 (AD45)
CAMERA_CLKREQ_L — PCIECLKRQ3*/GPIO25 (T3)
NC_PCIE_CLK100M_GPUN — CLKOUT_PCIE_N4 (AF43)
NC_PCIE_CLK100M_GPUP — CLKOUT_PCIE_P4 (AF45)
TBT_CLKREQ_L — PCIECLKRQ4*/GPIO26 (V3)
NC_PCIE_CLK100M_PE5N — CLKOUT_PCIE_N5 (AE44)
NC_PCIE_CLK100M_PE5P — CLKOUT_PCIE_P5 (AE42)
PCH_CLKRQ5_L_GPIO44 — PCIECLKRQ5*/GPIO44 (IPU-RSMRST#) (AA2)
NC_PCIE_CLK100M_SWN — CLKOUT_PCIE_N6 (AB40)
NC_PCIE_CLK100M_SWP — CLKOUT_PCIE_P6 (AB39)
PEG_CLKREQ_L — PCIECLKRQ6*/GPIO45 (AE4)
PCIE_CLK100M_TBT_N — CLKOUT_PCIE_N7 (AJ44)
PCIE_CLK100M_TBT_P — CLKOUT_PCIE_P7 (AJ42)
PCH_CLKRQ7_L_GPIO46 — PCIECLKRQ7*/GPIO46 (IPU-RSMRST#) (Y3)
NC_ITPXDP_CLK100MN — CLKOUT_ITPXDP_N (AH43)
NC_ITPXDP_CLK100MP — CLKOUT_ITPXDP_P (AH45)
LPC_CLK33M_SMC_R — CLKOUT_33MHZ0 (IPD-PWROK) (D44)
NC_LPC_CLK33M_LPCPLUS_R — CLKOUT_33MHZ1 (IPD-PWROK) (E44)
NC_PCI_CLK33M_OUT2 — CLKOUT_33MHZ2 (IPD-PWROK) (B42)
NC_PCI_CLK33M_OUT3 — CLKOUT_33MHZ3 (IPD-PWROK) (F41)
PCH_CLK33M_PCIOUT — CLKOUT_33MHZ4 (IPD-PWROK) (A40)

CLKOUT_PEG_A_N AB35 NC_PCIE_CLK100M_ENETN
CLKOUT_PEG_A_P AB36 NC_PCIE_CLK100M_ENETP
PEG_A_CLKRQ*/GPIO47 AF6 — ENET_CLKREQ_L
CLKOUT_PEG_B_N Y39 NC_PCIE_CLK100M_PEGBN
CLKOUT_PEG_B_P Y38 NC_PCIE_CLK100M_PEGBP
PEG_B_CLKRQ*/GPIO56 U4 — PCH_PEGCLKRQB_L_GPIO56
CLKOUT_DMI_N AF39 DMI_CLK100M_CPU_N
CLKOUT_DMI_P AF40 DMI_CLK100M_CPU_P
CLKOUT_DP_N AJ40 CPU_CLK135M_DPLLSS_N
CLKOUT_DP_P AJ39 CPU_CLK135M_DPLLSS_P
CLKOUT_DPNS_N AF35 CPU_CLK135M_DPLLREF_N
CLKOUT_DPNS_P AF36 CPU_CLK135M_DPLLREF_P
CLKIN_DMI_N AY24 PCIE_CLK100M_PCH_N
CLKIN_DMI_P AW24 PCIE_CLK100M_PCH_P
CLKIN_GND_N AR24 PCH_CLKIN_GNDN
CLKIN_GND_P AT24 PCH_CLKIN_GNDP
CLKIN_DOT96_N H33 PCH_CLK96M_DOT_N
CLKIN_DOT96_P G33 PCH_CLK96M_DOT_P
CLKIN_SATA_N BE6 PCH_CLK100M_SATA_N
CLKIN_SATA_P BC6 PCH_CLK100M_SATA_P
REFCLK14IN F45 PCH_CLK14P3M_REFCLK
CLKIN_33MHZLOOPBACK D17 PCH_CLK33M_PCIIN
XTAL25_IN AM43 SYSCLK_CLK25M_SB_R
XTAL25_OUT AL44 NC
(IPD-PWROK) CLKOUTFLEX0/GPIO64 C40 NC_PCH_GPIO64_CLKOUTFLEX0
(IPD-PWROK) CLKOUTFLEX1/GPIO65 F38 NC_PCH_GPIO65_CLKOUTFLEX1
(IPD-PWROK) CLKOUTFLEX2/GPIO66 F36 NC_PCH_GPIO66_CLKOUTFLEX2
(IPD-PWROK) CLKOUTFLEX3/GPIO67 F39 NC_PCH_GPIO67_CLKOUTFLEX3
ICLK_IREF AM45 — PP1V5_S0
TP19 AD39 NC
TP18 AD38 NC
DIFFCLK_BIASREF AN44 — PCH_DIFFCLK_BIASREF — R1190 7.5K 1% 1/20W MF 201 — PP1V5_S0
PLACE_NEAR=U1100.AN44:2.54mm

Unused clock terminations for FCIM Mode

R1196 10K — PCIE_CLK100M_PCH_N
R1195 10K — PCIE_CLK100M_PCH_P
R1171 10K — PCH_CLKIN_GNDN
R1170 10K — PCH_CLKIN_GNDP
R1192 10K — PCH_CLK96M_DOT_N
R1191 10K — PCH_CLK96M_DOT_P
R1194 10K — PCH_CLK100M_SATA_N
R1193 10K — PCH_CLK100M_SATA_P
R1197 10K — PCH_CLK14P3M_REFCLK
5% 1/20W MF 201

R1172 340 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB
1.5V -> 1.1V
R1173 1K 1% 1/20W MF 201

PPVRTC_G3H
R1100 330K 5% 1/20W MF 201
R1101 1M 5% 1/20W MF 201
R1102 20K 5% 1/20W MF 201
R1103 20K 5% 1/20W MF 201
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
C1102 1UF 10% 10V X5R 402
C1103 1UF 10% 10V X5R 402

NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

PP3V3_SUS
PP3V3_S0

R1177 4.7K — PCH_SPKR
R1176 10K — DP_TBT_SEL
R1178 4.7K — PCH_SATALED_L
R1134 10K — DP_AUXCH_ISOL_L
R1133 10K — XDP_DC1_SATARDRVR_EN
R1143 10K — SSD_CLKREQ_L
R1142 10K — XDP_DD2_ENETSD_CLKREQ_L
R1169 10K — AP_CLKREQ_L
R1144 10K — CAMERA_CLKREQ_L
R1145 10K — TBT_CLKREQ_L
R1147 10K — PCH_CLKRQ5_L_GPIO44
R1114 10K — PEG_CLKREQ_L
R1115 10K — PCH_CLKRQ7_L_GPIO46
R1146 10K — ENET_CLKREQ_L
R1148 10K — PCH_PEGCLKRQB_L_GPIO56
R1179 10K — ENET_MEDIA_SENSE_RDIV
5% 1/20W MF 201

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK

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OMIT_TABLE

U1100
LYNXPOINT MOBILE
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DMI_RXN0 AW22 ← DMI_N2S_N<0>
DMI_RXN1 AR20 ← DMI_N2S_N<1>
DMI_RXN2 AP17 ← DMI_N2S_N<2>
DMI_RXN3 AV20 ← DMI_N2S_N<3>
DMI_RXP0 AY22 ← DMI_N2S_P<0>
DMI_RXP1 AP20 ← DMI_N2S_P<1>
DMI_RXP2 AR17 ← DMI_N2S_P<2>
DMI_RXP3 AW20 ← DMI_N2S_P<3>
DMI_TXN0 BD21 → DMI_S2N_N<0>
DMI_TXN1 BE20 → DMI_S2N_N<1>
DMI_TXN2 BD17 → DMI_S2N_N<2>
DMI_TXN3 BE18 → DMI_S2N_N<3>
DMI_TXP0 BB21 → DMI_S2N_P<0>
DMI_TXP1 BC20 → DMI_S2N_P<1>
DMI_TXP2 BB17 → DMI_S2N_P<2>
DMI_TXP3 BC18 → DMI_S2N_P<3>
DMI_IREF BE16 ← PP1V5_S0 via R1200 7.5K 1% 1/20W MF 201 (PLACE_NEAR=U1100.AY17:12.7mm)
TP12 AW17 → NC
TP7 AV17 → NC
DMI_RCOMP AY17 ← PCH_DMI_RCOMP

FDI_RXN0 AJ35 → NC
FDI_RXN1 AL35 → NC
FDI_RXP0 AJ36 → NC
FDI_RXP1 AL36 → NC
TP16 AV43 → NC
TP5 AY45 → NC
TP15 AV45 → NC
TP10 AW44 → NC
FDI_CSYNC AL39 ← FDI_CSYNC
FDI_INT AL40 ← FDI_INT
FDI_IREF AT45 ← PP1V5_S0 via R1210 7.5K 1% 1/20W MF 201 (PLACE_NEAR=U1100.AR44:12.7mm)
TP17 AU42 → NC
TP13 AU44 → NC
FDI_RCOMP AR44 ← PCH_FDI_RCOMP

PP1V5_S0 → R1210 7.5K → PPVRTC_G3H → R1215 330K 5% 1/20W MF 201
PPVRTC_G3H → R1209 100K 5% 1/20W MF 201

SYSTEM POWER MANAGEMENT

SUSACK* (IPU) R6 ← PCH_SUSACK_L
SYS_RESET* AM1 ← PM_SYSRST_L
SYS_PWROK AD7 ← PM_PCH_SYS_PWROK
PWROK F10 ← PM_PCH_PWROK
APWROK AB7 ← PM_PCH_PWROK
DRAMPWROK (OD) H3 ← PM_MEM_PWRGD
RSMRST* J2 ← PM_RSMRST_L
SUSWARN*/SUSPWRNACK/GPIO30 J4 → PCH_SUSWARN_L
PWRBTN* (IPU) K1 ← PM_PWRBTN_L
ACPRESENT/GPIO31 (IPD-DeepSx) E6 ← SMC_ADAPTER_EN
BATLOW*/GPIO72 K7 ← PM_BATLOW_L
RI* N4 ← PCH_RI_L
TP21 AB10 ← TP_PCH_SLP_S0_L
SLP_WLAN*/GPIO29 D2 ← TP_PCH_SLP_WLAN_L

DSWVRMEN C8 ← PCH_DSWVRMEN
DPWROK L13 ← PM_DSW_PWRGD
WAKE* (IPD-DeepSx) K3 → PCIE_WAKE_L
CLKRUN* AN7 ↔ PM_CLKRUN_L
SUS_STAT*/GPIO61 U7 → LPC_PWRDWN_L
SUSCLK/GPIO62 (IPU-RSMRST#) Y6 → PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63 Y7 → PM_SLP_S5_L
SLP_S4* C6 → PM_SLP_S4_L
SLP_S3* H1 → PM_SLP_S3_L
SLP_A* F3 → TP_PM_SLP_A_L
SLP_SUS* F1 → PM_SLP_SUS_L
PMSYNCH AY3 → PM_SYNC
SLP_LAN* G5 → PM_PCH_SLP_LAN_L

SMC_SUSACK:NO
R1286 0 5% 1/20W MF 0201
PP3V3_SUS → R1205 10K 5% 1/20W MF 201
NO STUFF: R1287 10K 5% 1/20W MF 201

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(5 OF 11)

VGA_BLUE T45 → NC
VGA_GREEN U44 → NC
VGA_RED V45 → NC
VGA_DDC_CLK M43 → NC
VGA_DDC_DATA M45 → NC
VGA_HSYNC N42 → NC
VGA_VSYNC N44 → NC
DAC_IREF U40 ← PP3V3_S0 via R1260 10K 5% 1/20W MF 201
VGA_IRTN U39 → GND

VGA DAC Disabled per SB DG v1.0 (Table 12-18).

DDPB_CTRLCLK R40 → DP_TBTSNK0_DDC_CLK
DDPB_CTRLDATA (IPD-PLTRST#) R39 → DP_TBTSNK0_DDC_DATA
DDPC_CTRLCLK R35 → DP_TBTSNK1_DDC_CLK
DDPC_CTRLDATA (IPD-PLTRST#) R36 → DP_TBTSNK1_DDC_DATA
DDPD_CTRLCLK N40 → HDMI_DDC_CLK
DDPD_CTRLDATA (IPD-PLTRST#) N38 → HDMI_DDC_DATA
DDPB_AUXN H45 → DP_TBTSNK0_AUXCH_C_N
DDPC_AUXN K43 → DP_TBTSNK1_AUXCH_C_N
DDPD_AUXN J42 → NC_DP_IG_D_AUXCHN
DDPB_AUXP H43 → DP_TBTSNK0_AUXCH_C_P
DDPC_AUXP K45 → DP_TBTSNK1_AUXCH_C_P
DDPD_AUXP J44 → NC_DP_IG_D_AUXCHP
DDPB_HPD K40 ← DP_TBTSNK0_HPD
DDPC_HPD K38 ← DP_TBTSNK1_HPD
DDPD_HPD H39 ← HDMI_HPD

CRT
DISPLAY
EDP
PCI

EDP_BKLTCTL N36 ← EDP_IG_BKL_PWM
EDP_BKLTEN K36 ← EDP_IG_BKL_ON
EDP_VDDEN G36 ← EDP_IG_PANEL_PWR

PIRQA* H20 ← PCI_INTA_L
PIRQB* L20 ← PCI_INTB_L
PIRQC* K17 ← PCI_INTC_L
PIRQD* M20 ← PCI_INTD_L
GPIO50 A12 ← ENET_LOW_PWR_PCH
GPIO52 B13 ← AUD_IPHS_SWITCH_EN_PCH
GPIO54 C12 ← BT_PWRRST_L
GPIO51 C10 ← TP_PCH_STRP_BBS1
GPIO53 A10 ← TP_PCH_STRP_ESI_L
GPIO55 AL6 ← PCH_STRP_TOPBLK_SWP_L
(IPU-PWROK&PCIRST#)

PIRQE*/GPIO2 G17 → SDCONN_OC_L
PIRQF*/GPIO3 F17 → AUD_IP_PERIPHERAL_DET
PIRQG*/GPIO4 L15 → TBT_PWR_REQ_L
PIRQH*/GPIO5 M15 → AUD_I2C_INT_L
(IPU) PME* AD10 → NC_PCI_PME_L
PLTRST* Y11 → PLT_RESET_L

PP3V3_S5
PP3V3_S0

R1239 3.0K PM_PWRBTN_L
R1240 10K PM_BATLOW_L
R1291 10K PM_CLKRUN_L
R1216 10K ENET_LOW_PWR_PCH
R1217 100K AUD_IPHS_SWITCH_EN_PCH
R1218 10K BT_PWRRST_L
R1230 10K SDCONN_OC_L
NO STUFF Redundant to pull-up on audio page
R1214 100K AUD_IP_PERIPHERAL_DET
R1231 10K TBT_PWR_REQ_L
NO STUFF Redundant to pull-up on audio page
R1233 10K AUD_I2C_INT_L
R1225 1K PCIE_WAKE_L
R1224 100K PM_SLP_S3_L
R1221 100K PM_SLP_S4_L
R1222 100K PM_SLP_S5_L
R1223 100K PM_SLP_SUS_L
R1281 100K EDP_IG_BKL_ON
R1284 100K EDP_IG_PANEL_PWR

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 12 OF 118
SHEET: 12 OF 82

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(9 OF 11)

USB3 Port Assignments:

Unused

PCIe/USB3 Port Assignments:

SD Card Reader
(& Ethernet if combo)

PCIe Port Assignments:

AirPort

Camera

SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD

73	NC_USB3_SPARE_D2RN	AW31	PERN1_USB3RN3
73	NC_USB3_SPARE_D2RP	AY31	PERP1_USB3RP3
73	NC_USB3_SPARE_R2D_CN	BE32	PETN1_USB3TN3
73	NC_USB3_SPARE_R2D_CP	BC32	PETP1_USB3TP3
77 72 69 20	IN USB3_SD_D2R_N	AT31	PERN2_USB3RN4
77 72 69 20	IN USB3_SD_D2R_P	AR31	PERP2_USB3RP4
77 72 69 20	OUT USB3_SD_R2D_C_N	BD33	PETN2_USB3TN4
77 72 69 20	OUT USB3_SD_R2D_C_P	BB33	PETP2_USB3TP4
77 34	IN PCIE_AP_D2R_N	AW33	PERN3
77 34	IN PCIE_AP_D2R_P	AY33	PERP3
77 34	OUT PCIE_AP_R2D_C_N	BE34	PETN3
77 34	OUT PCIE_AP_R2D_C_P	BC34	PETP3
77 37	IN PCIE_CAMERA_D2R_N	AT33	PERN4
77 37	IN PCIE_CAMERA_D2R_P	AR33	PERP4
77 37	OUT PCIE_CAMERA_R2D_C_N	BE36	PETN4
77 37	OUT PCIE_CAMERA_R2D_C_P	BC36	PETP4
71	IN NC_PCIE_SSD_D2RN<0>	AW36	PERN5
71	IN NC_PCIE_SSD_D2RP<0>	AV36	PERP5
71	OUT NC_PCIE_SSD_R2D_CN<0>	BD37	PETN5
71	OUT NC_PCIE_SSD_R2D_CP<0>	BB37	PETP5
71	IN NC_PCIE_SSD_D2RN<1>	AY38	PERN6
71	IN NC_PCIE_SSD_D2RP<1>	AW38	PERP6
71	OUT NC_PCIE_SSD_R2D_CN<1>	BC38	PETN6
71	OUT NC_PCIE_SSD_R2D_CP<1>	BE38	PETP6
71	IN NC_PCIE_SSD_D2RN<2>	AT40	PERN7
71	IN NC_PCIE_SSD_D2RP<2>	AT39	PERP7
71	OUT NC_PCIE_SSD_R2D_CN<2>	BE40	PETN7
71	OUT NC_PCIE_SSD_R2D_CP<2>	BC40	PETP7
71	IN NC_PCIE_SSD_D2RN<3>	AN38	PERN8
71	IN NC_PCIE_SSD_D2RP<3>	AN39	PERP8
71	OUT NC_PCIE_SSD_R2D_CN<3>	BD42	PETN8
71	OUT NC_PCIE_SSD_R2D_CP<3>	BD41	PETP8
		BE30	PCIE_IREF
		BC30	TP11
		BB29	TP6
		BD29	PCIE_RCOMP

PP1V5_S0 — R1300 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.BD29:12.7mm — PCH PCIE RCOMP

USB Port Assignments:

USB2N0	B37	USB_EXTA_N	B1	38 76
USB2P0	D37	USB_EXTA_P	B1	38 76
USB2N1	A38	NC_USB_EXTCN	B1	73 76
USB2P1	C38	NC_USB_EXTCP	B1	73 76
USB2N2	A36	NC_USB_SDN		73 76
USB2P2	C36	NC_USB_SDP		73 76
USB2N3	A34	NC_USB_WLANN		73
USB2P3	C34	NC_USB_WLANP		73
USB2N4	B33	NC_USB_4N		73
USB2P4	D33	NC_USB_4P		73
USB2N5	F31	NC_USB_PSOCN		73
USB2P5	G31	NC_USB_PSOCP		73
USB2N6	K31	NC_USB_6N		73 76
USB2P6	L31	NC_USB_6P		73 76
USB2N7	G29	NC_USB_7N		73 76
USB2P7	H29	NC_USB_7P		73 76
USB2N8	A32	USB_EXTB_N	B1	69 72 76
USB2P8	C32	USB_EXTB_P	B1	69 72 76
USB2N9	A30	NC_USB_EXTDN	B1	73 76
USB2P9	C30	NC_USB_EXTDP	B1	73 76
USB2N10	B29	TP_USB_CAMERAN		
USB2P10	D29	TP_USB_CAMERAP		
USB2N11	A28	USB_BT_N	B1	34 76
USB2P11	C28	USB_BT_P	B1	34 76
USB2N12	G26	NC_USB_IRN	B1	73 76
USB2P12	F26	NC_USB_IRP	B1	73 76
USB2N13	F24	USB_TPAD_N	B1	39 72 76
USB2P13	G24	USB_TPAD_P	B1	39 72 76

(IPD)

USB3 Port Assignments:

USB3RN1	AR26	USB3_EXTA_D2R_N	IN	38 76
USB3RP1	AP26	USB3_EXTA_D2R_P	IN	38 76
USB3TN1	BE24	USB3_EXTA_R2D_C_N	OUT	38 76
USB3TP1	BD23	USB3_EXTA_R2D_C_P	OUT	38 76
USB3RN2	AW26	USB3_EXTB_D2R_N	IN	69 72 76
USB3RP2	AV26	USB3_EXTB_D2R_P	IN	69 72 76
USB3TN2	BD25	USB3_EXTB_R2D_C_N	OUT	69 76
USB3TP2	BC24	USB3_EXTB_R2D_C_P	OUT	69 76
USB3RN5	AW29	NC_USB3_EXTC_D2RN	IN	73 76
USB3RP5	AV29	NC_USB3_EXTC_D2RP	IN	73 76
USB3TN5	BE26	NC_USB3_EXTC_R2D_CN	OUT	73 76
USB3TP5	BC26	NC_USB3_EXTC_R2D_CP	OUT	73 76
USB3RN6	AR29	NC_USB3_EXTD_D2RN	IN	73 76
USB3RP6	AP29	NC_USB3_EXTD_D2RP	IN	73 76
USB3TN6	BD27	NC_USB3_EXTD_R2D_CN	OUT	73 76
USB3TP6	BE28	NC_USB3_EXTD_R2D_CP	OUT	73 76

USBRBIAS*	K24	76 PCH_USB_RBIAS	
USBRBIAS	K26		
TP24	M33	NC	
TP23	L33	NC	

PLACE_NEAR=U1100.K24:11.4mm — R1370 22.6 1% 1/20W MF 201

OC0*/GPIO59	P3	XDP_DA0_USB_EXTA_OC_L	IN 13 18
OC1*/GPIO40	V1	XDP_DA1_USB_EXTC_OC_L	IN 13 18
OC2*/GPIO41	U2	XDP_DA2_SSD_PWR_EN	OUT 18
OC3*/GPIO42	P1	XDP_DA3_CAMERA_PWR_EN	OUT 18
OC4*/GPIO43	M3	XDP_DB0_USB_EXTB_OC_L	IN 13 18
OC5*/GPIO9	T1	XDP_DB1_USB_EXTD_OC_L	IN 13 18
OC6*/GPIO16	N2	XDP_DB2_SD_PWR_EN	OUT 18
OC7*/GPIO14	M1	XDP_DB3_SDCONN_STATE_CHANGE_L	IN 13 18

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(3 OF 11)

77 41	B1 LPC_AD<0>	R1340 33	LPC_AD_R<0>	A20 LAD0 (IPU)
77 41	B1 LPC_AD<1>	R1341 33	LPC_AD_R<1>	C20 LAD1 (IPU)
77 41	B1 LPC_AD<2>	R1342 33	LPC_AD_R<2>	A18 LAD2 (IPU)
77 41	B1 LPC_AD<3>	R1343 33	LPC_AD_R<3>	C18 LAD3 (IPU)
77 41	OUT LPC_FRAME_L	R1344 33	LPC_FRAME_R_L	B21 LFRAME*
73			NC_LPC_DREQ0_L	D21 LDRQ0* (IPU)
20 13	OUT TBT_PWR_EN_PCH			G20 LDRQ1*/GPIO23 (IPD-LDRQ1#?)
41 13	B1 LPC_SERIRQ			AL11 SERIRQ

5% 1/20W MF 201

77 50	OUT SPI_CLK_R		AJ11 SPI_CLK
77 50	OUT SPI_CS0_R_L		AJ7 SPI_CS0* (IPU)
	TP_SPI_CS1_L		AL7 SPI_CS1* (IPU)
	TP_SPI_CS2_L		AJ10 SPI_CS2* (IPU)
77 50	B1 SPI_MOSI_R		AH1 SPI_MOSI (IPD)
77 50	B1 SPI_MISO		AH3 SPI_MISO (IPU)
77 50 13	B1 SPI_IO<2>		AJ4 SPI_IO2 (IPU)
77 50 13	B1 SPI_IO<3>		AJ2 SPI_IO3 (IPU)

SMBALERT*/GPIO11	N7	PCH_SMBALERT_L	13
SMBCLK	R10	SMBUS_PCH_CLK	OUT 18 44 69 71 72 77
SMBDATA	U11	SMBUS_PCH_DATA	B1 18 44 69 71 72 77
SML0ALERT*/GPIO60	N8	PCH_SML0ALERT_L	13
SML0CLK	U8	SML_PCH_0_CLK	OUT 44 77
SML0DATA	R7	SML_PCH_0_DATA	B1 44 77
SML1ALERT*/PCHHOT*/GPIO74	H6	PCH_SML1ALERT_L	13
SML1CLK/GPIO58	K6	SML_PCH_1_CLK	IN 44 77
SML1DATA/GPIO75	N11	SML_PCH_1_DATA	B1 44 77
(IPU/IPD) CL_CLK	AF11	NC_CLINK_CLK	73
(IPU/IPD) CL_DATA	AF10	NC_CLINK_DATA	73
CL_RST*	AF7	NC_CLINK_RESET_L	73
TP1	BA45	NC	
TP2	BC45	NC	
TP4	BE43	NC	
TP3	BE44	NC	
TD_IREF	AY43	PCH_TD_IREF	

R1380 0.2K 1% 1/20W MF 201

PP3V3_SUS
PP3V3_SUS
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0

R1350	10K	LPC_SERIRQ	13 41
R1351	10K	TBT_PWR_EN_PCH	13 20
R1360	10K	XDP_DA0_USB_EXTA_OC_L	13 18
R1361	10K	XDP_DA1_USB_EXTC_OC_L	13 18
R1362	10K	SSD_PWR_EN	18 66
R1368	10K	CAMERA_PWR_EN	18 36
R1320	10K	XDP_DB0_USB_EXTB_OC_L	13 18
R1321	10K	XDP_DB1_USB_EXTD_OC_L	13 18
R1367	10K	SD_PWR_EN	18 69 72
R1369	10K	XDP_DB3_SDCONN_STATE_CHANGE_L	13 18
R1392	1K	SPI_IO<2>	13 50 77
R1393	1K	SPI_IO<3>	13 50 77
R1353	10K	PCH_SMBALERT_L	13
R1354	10K	PCH_SML0ALERT_L	13
R1355	10K	PCH_SML1ALERT_L	13

5% 1/20W MF 201

SYNC_MASTER=J15_REFERENCE — SYNC_DATE=12/18/2012

PAGE TITLE: PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 13 OF 118
SHEET: 13 OF 82

Pull-up/down on chipset support page (depends on TBT controller)
Falcon Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(6 OF 11)

TBT_CIO_PLUG_EVENT_L	AT8	BMBUSY*/GPIO0	
FW_PME_L	F13	TACH1/GPIO1	
DPMUX_UC_IRQ	A14	TACH2/GPIO6	
SMC_RUNTIME_SCI_L	G15	TACH3/GPIO7	
XDP_FC0_HDD_PWR_EN	Y1	GPIO8 (IPU-RSMRST#)	
WOL_EN	K13	LAN_PHY_PWR_CTRL/GPIO12	
MEM_VDD_SEL_1V5_L	AB11	GPIO15	
XDP_DD0_SSD_PCIE_SEL_L	AN2	SATA4GP/GPIO16 (IPU-BOOT/SATA4GP?)	
LPCPLUS_GPIO	C14	TACH0/GPIO17	
JTAG_TBT_TMS_PCH	BB4	SCLOCK/GPIO22	
TBT_GO2SX_BIDIR	Y10	GPIO24	
SMC_WAKE_SCI_L	R11	GPIO27 (IPU-DeepSx)	
ISOLATE_CPU_MEM_L	AD11	GPIO28	
TBT_POC_RESET_L	AN6	GPIO34	
XDP_FC1_GPU_GOOD	AP1	GPIO35/NMI*	
XDP_DC2_ODD_PWR_EN_L	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)	
XDP_DC3_JTAG_ISP_TCK	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)	
JTAG_ISP_TDO	AT7	SLOAD/GPIO38	
JTAG_ISP_TDI	AM3	SDATAOUT0/GPIO39	
FW_PWR_EN_PCH	AN4	SDATAOUT1/GPIO48	
XDP_DD1_MLB_RAMCFG1	AK3	SATA5GP/GPIO49 (IPD-BOOt/SATA5GP?)	
SPIROM_USE_MLB	U12	GPIO57	
MLB_RAMCFG3	C16	TACH4/GPIO68	
MLB_RAMCFG2	D13	TACH5/GPIO69	
SD_SEL_PCIE_L_USB_H	G13	TACH6/GPIO70 (IPU-BOot?)	
MLB_RAMCFG0	H15	TACH7/GPIO71 (IPU-BOot?)	

CPU/MISC
GPIO

	BE41	VSS	
	BE5		
	C45		
	A5		

TP14	AN10	PCH_A20GATE	14
(IPD) PECI	AY1	PCH_PECI	
RCIN*	AT6	PCH_RCIN_L	14 77
PROCPWRGD	AV3	PCH_PROCPWRGD	
THRMTRIP*	AV1	PM_THRMTRIP_L_R	42 42
PLTRST_PROC*	AU4	CPU_RESET_L	OUT 6
VSS	N10		

	A2	
	A41	
	A43	
	A44	
	B1	
	B2	
	B44	
	B45	
	BA1	
	BC1	
	BD1	
	BD2	
VSS	BD44	
	BD45	
	BE2	
	BE3	
	D1	
	E1	
	E45	
	A4	

PP1V05_S0
BDW_SPRT
R1457 1K 5% 1/16W MF-LF 402

R1470 43 NO STUFF 5% 1/20W MF 201 — CPU_PECI (BI) 6 42 75
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD (OUT) 6 18 75
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L (IN) 6 42 75
CRW_SPRT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R1456		BDW_SPRT

PP3V3_S0

RAMCFG0:H R1475 10K 5% 1/20W MF 201
RAMCFG1:H R1474 10K 5% 1/20W MF 201
RAMCFG2:H R1473 10K 5% 1/20W MF 201
RAMCFG3:H R1472 10K 5% 1/20W MF 201

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	FW_PME_L	14 71
R1411	20K	DPMUX_UC_IRQ	14 71
R1496	10K	SMC_RUNTIME_SCI_L	14 41
R1494	10K	WOL_EN	14 71
R1489	10K	MEM_VDD_SEL_1V5_L	14 71
R1495	100K	XDP_DD0_SSD_PCIE_SEL_L	14 18
R1490	100K	LPCPLUS_GPIO	14 71
R1412	10K	JTAG_TBT_TMS_PCH	14 20
R1492	10K	TBT_GO2SX_BIDIR	14 71
R1491	10K	SMC_WAKE_SCI_L	14 41
R1498	10K	XDP_DC2_ODD_PWR_EN_L	14 18
R1413	10K	JTAG_ISP_TCK	18 20
R1486	10K	JTAG_ISP_TDO	14 20
R1499	10K	JTAG_ISP_TDI	14 20
R1484	10K	FW_PWR_EN_PCH	14 71
R1493	100K	SPIROM_USE_MLB	14 50 72

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	PCH_A20GATE	14
R1455	10K	PCH_RCIN_L	14 77

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014
PAGE TITLE: PCH GPIO/MISC/NCTF
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
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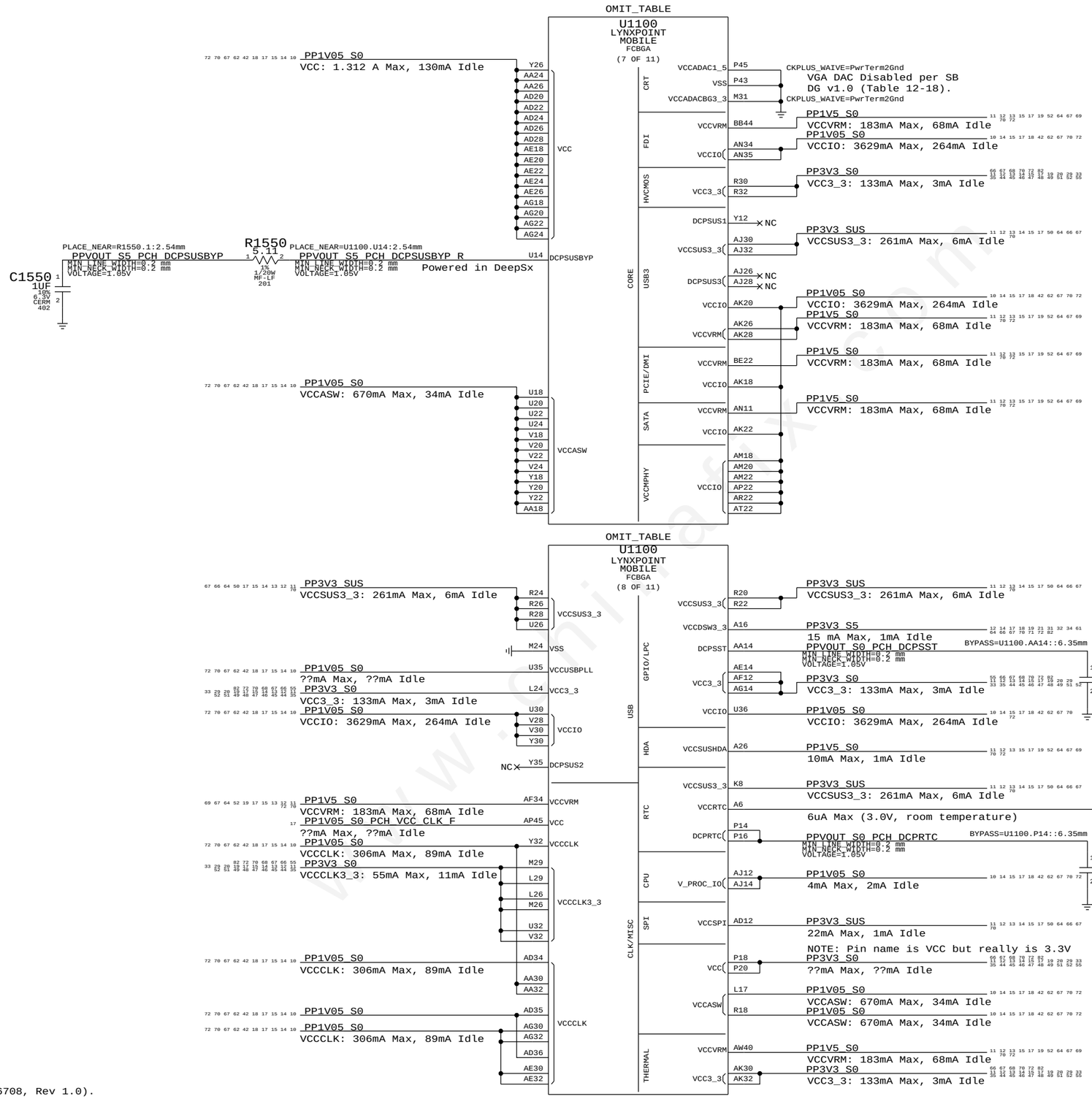

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Power

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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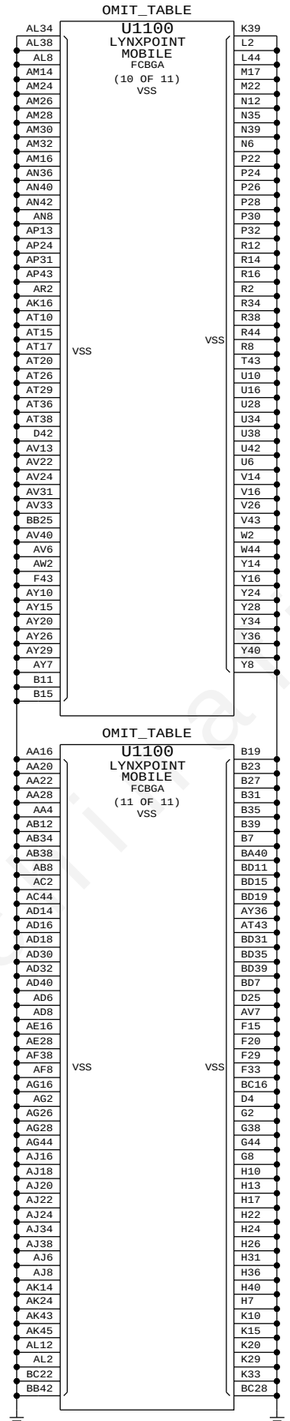

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 20% 10V CERM 402
BYPASS=U1100.R20::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 20% 10V CERM 402
BYPASS=U1100.R26::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8::6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26::6.35mm
BYPASS=U1100.L29::6.35mm
BYPASS=U1100.M29::6.35mm
BYPASS=U1100.U32::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.R30::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 20% 10V CERM 402
BYPASS=U1100.L24::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK30::6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18::6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18::12.7mm
BYPASS=U1100.AG22::6.35mm
BYPASS=U1100.AD20::6.35mm
BYPASS=U1100.AE18::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18::12.7mm
BYPASS=U1100.AK22::6.35mm
BYPASS=U1100.AK20::6.35mm
BYPASS=U1100.AM18::6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30::6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12::12.7mm
BYPASS=U1100.AJ12::6.35mm
BYPASS=U1100.AJ12::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30::6.35mm
BYPASS=U1100.AG30::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26::6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34::12.7mm

PP1V05_S0
??mA Max, ??mA Idle
R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603

PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45::12.7mm
BYPASS=U1100.AP45::6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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PCH DECOUPLING

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807
(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU
PP1V05_S0
R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	XDP_CPU_PRESENT_L

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

R1805 1K 5% 1/20W MF 201 XDP
XDP_PLT_RESET_L → PLACE_NEAR=U0500.AG7:2.54mm

CPU_PWRGD — R1800 1K 5% 1/20W MF 201 — PLACE_NEAR=U0500.F50:2.54mm
PM_PWRBTN_L — R1802 0 5% 1/20W MF 0201 — PLACE_NEAR=U5000.J3:2.54mm
PM_PCH_SYS_PWROK — R1804 0 5% 1/16W MF-LF 402

R1820 51 5% 1/20W MF 201 — XDP_CPU_TDO — PLACE_NEAR=U0500.M49:28mm
R1823 51 5% 1/20W MF 201 — XDP_CPU_TCK — PLACE_NEAR=U0500.N54:28mm
R1824 51 5% 1/20W MF 201 — XDP_CPUPCH_TRST_L — PLACE_NEAR=U0500.M53:28mm

TDI and TMS are terminated in CPU.

CRITICAL Q1840 DMN5L06VK-7 SOT563 VER 5 — XDP_CPU_TDO — PLACE_NEAR=J1800.51:28mm
CRITICAL Q1840 DMN5L06VK-7 SOT563 VER 5 — XDP_CPUPCH_TRST_L — PLACE_NEAR=J1800.53:28mm — MAKE_BASE=TRUE
CRITICAL Q1842 DMN5L06VK-7 SOT563 VER 5 — XDP_CPU_TDI — PLACE_NEAR=J1800.55:28mm
CRITICAL Q1842 DMN5L06VK-7 SOT563 VER 5 — XDP_CPU_TMS — PLACE_NEAR=J1800.57:28mm

PCH/XDP Signals

OMIT (All 10 R's)

			Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L	R1890	SHORT	USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT	SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT	CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT	USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT	SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT	SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT	DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN	MAKE_BASE=TRUE		XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L	MAKE_BASE=TRUE		XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT	JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT	SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1	MAKE_BASE=TRUE		XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L	MAKE_BASE=TRUE		XDP_DD2_ENETSD_CLKREQ
XDP_DD3_AP_CLKREQ_L	R1879	SHORT	AP_CLKREQ_L

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813
(TP-P6)

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

XDP_PCH_TDO	R1860	51
XDP_PCH_TDI	R1861	51
XDP_PCH_TMS	R1862	51
XDP_PCH_TCK	R1866	51

5% 1/20W MF 201 — PLACE_NEAR=U1100.AD3:28mm / AE2:28mm / AD1:28mm / AB3:28mm

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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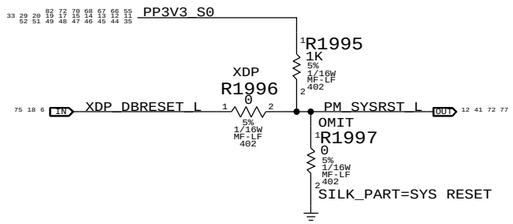
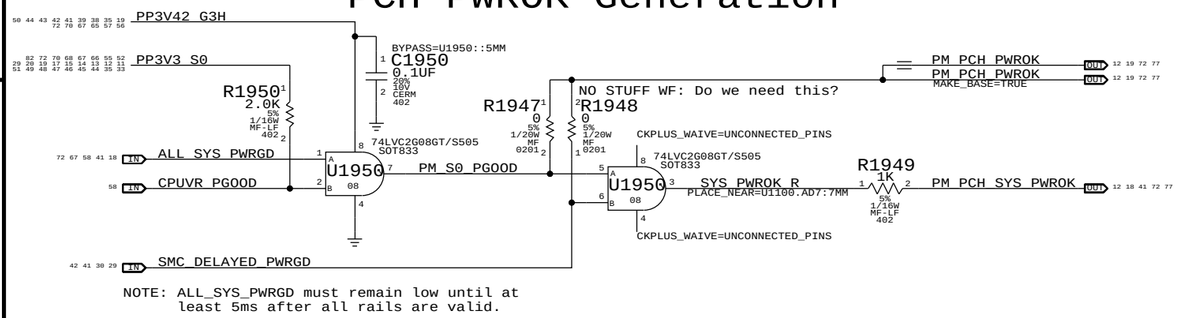
PCH Reset Button

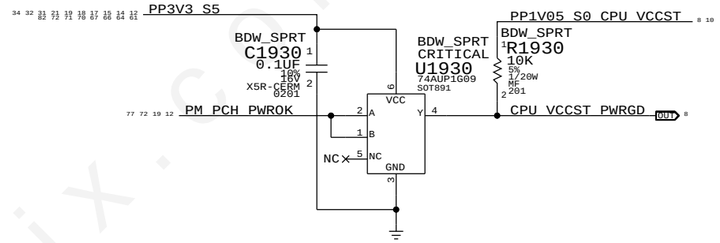


PCH PWROK Generation

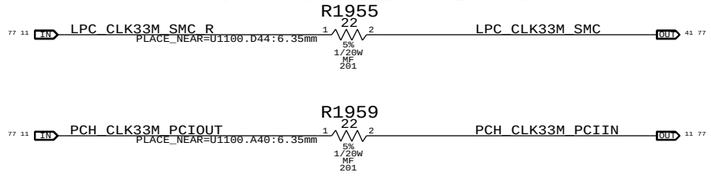


NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

VCCST (1.05V S0) PWRGD



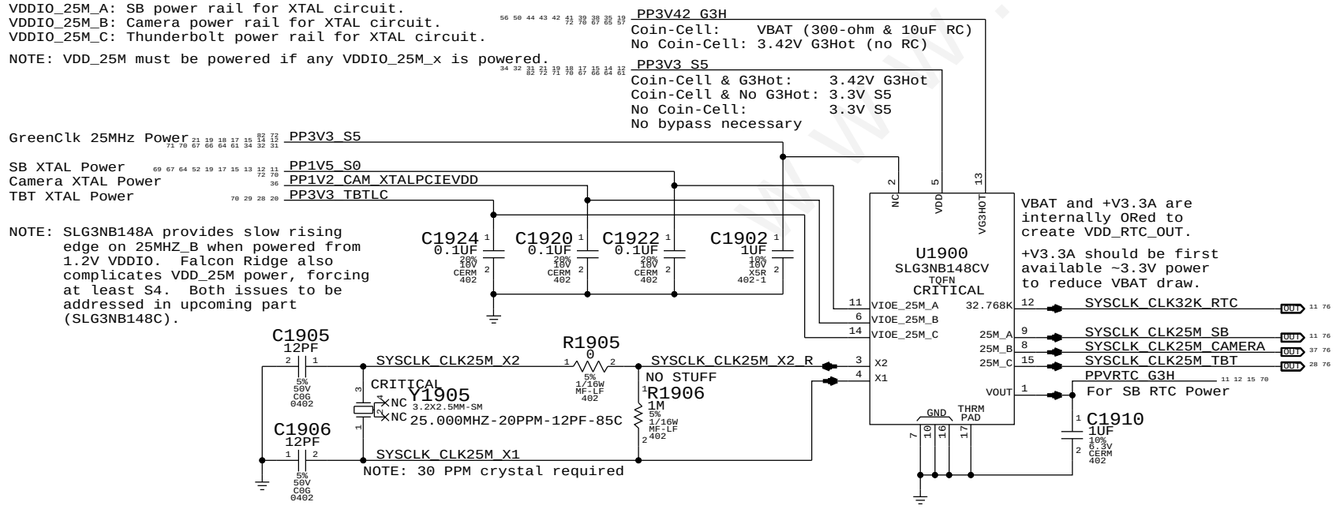
PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

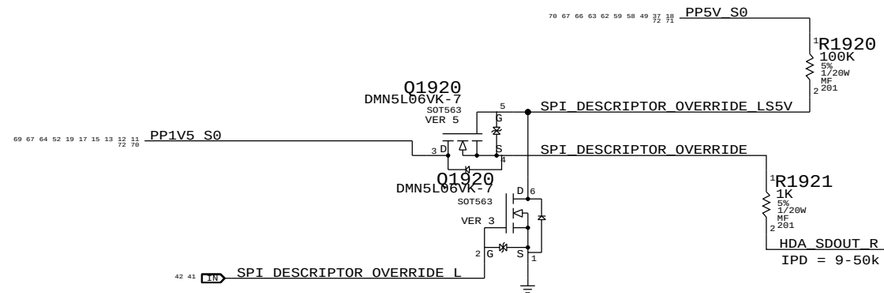


NOTE: 30 PPM crystal required

NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Falcon Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Chipset Support

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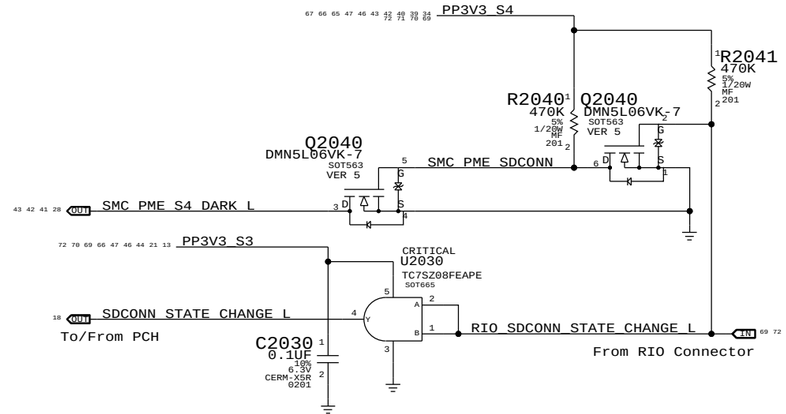
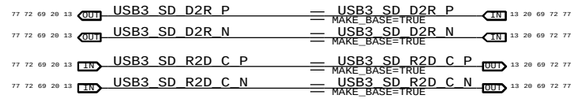
RIO SD Card Reader Support



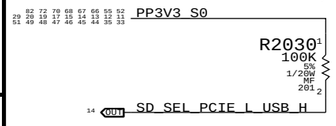
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



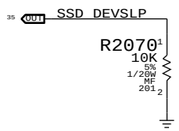
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe



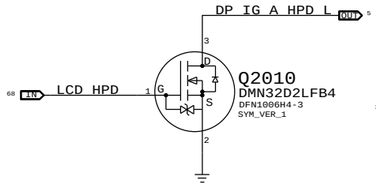
GS3 Connector Support

DEVSLP not supported on LPT-H

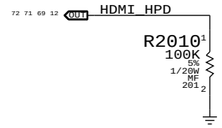


LCD HPD Inverter

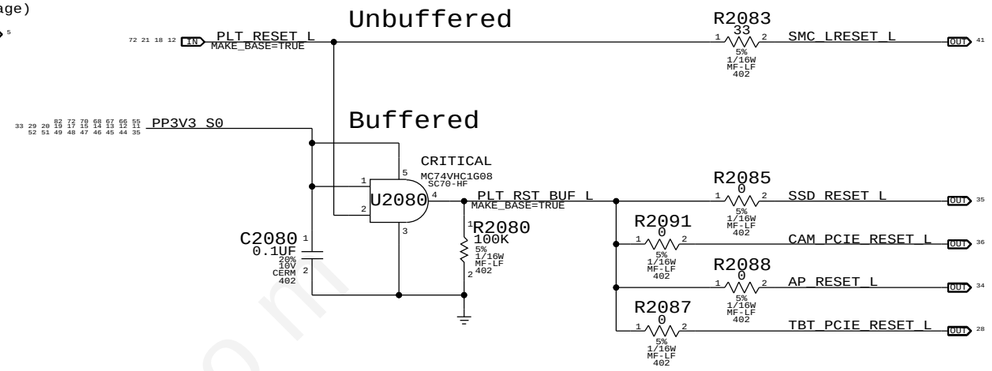
(Pull-Up on CPU Page)



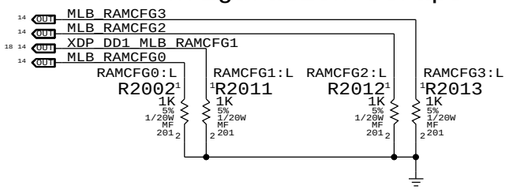
HDMI HPD pull-down



Platform Reset Connections

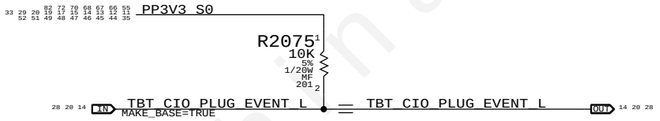


RAM Configuration Straps



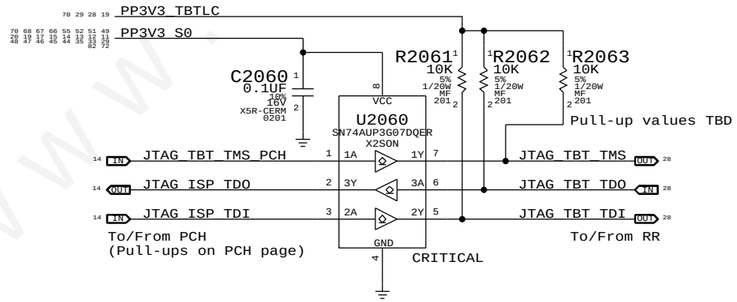
Falcon Ridge Support

RR output is open-drain, no isolation necessary

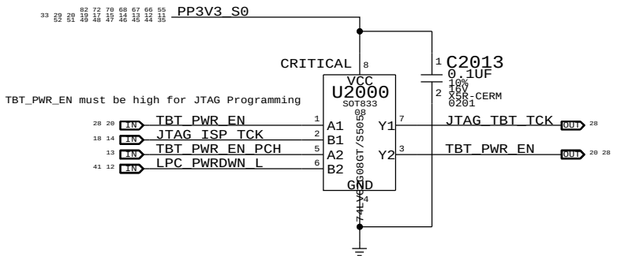


Falcon Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



GPIO Glitch Prevention



SYNC_MASTER=J15_REFERENCE	SYNC_DATE=01/14/2013
PAGE TITLE: Project Chipset Support	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
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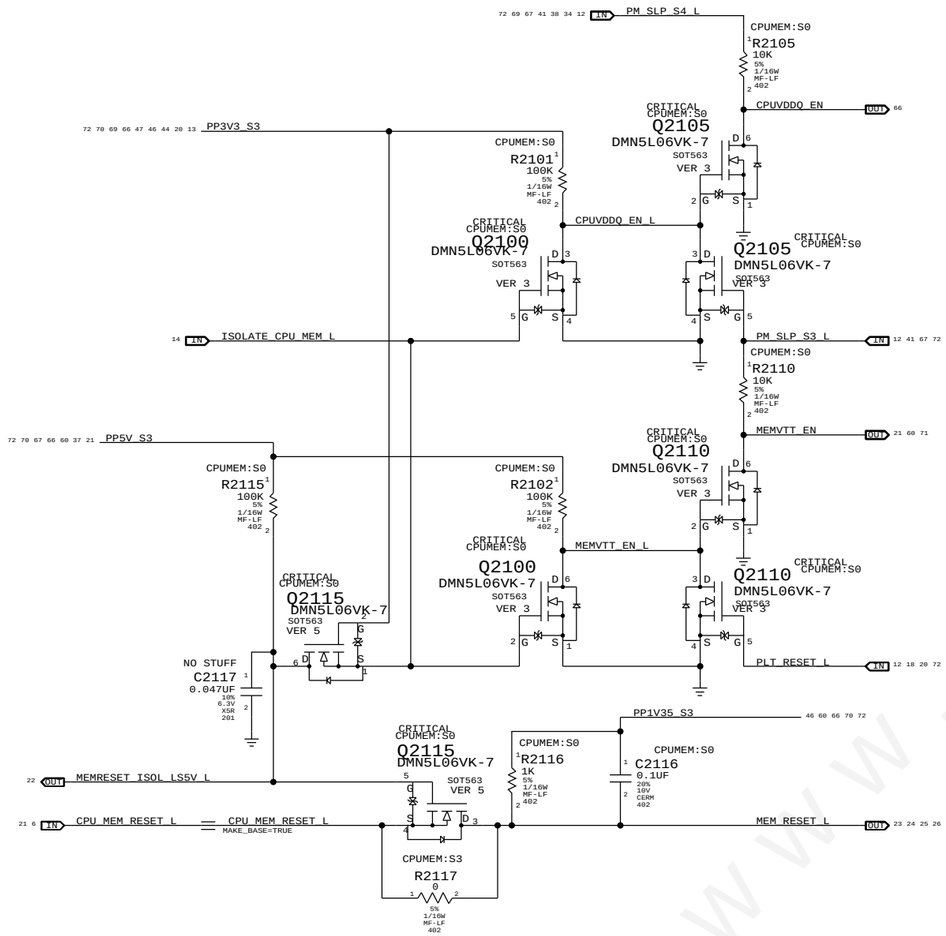
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



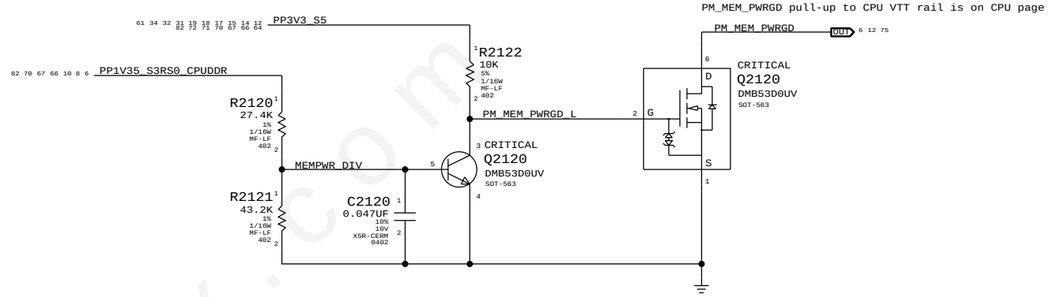
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

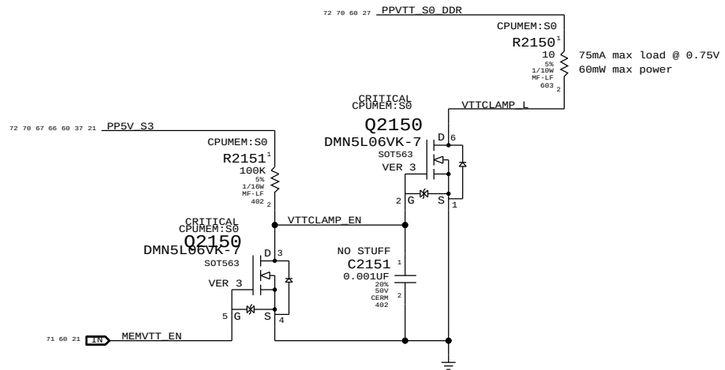
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=CLEAN_X305G SYNC_DATE=07/01/2014

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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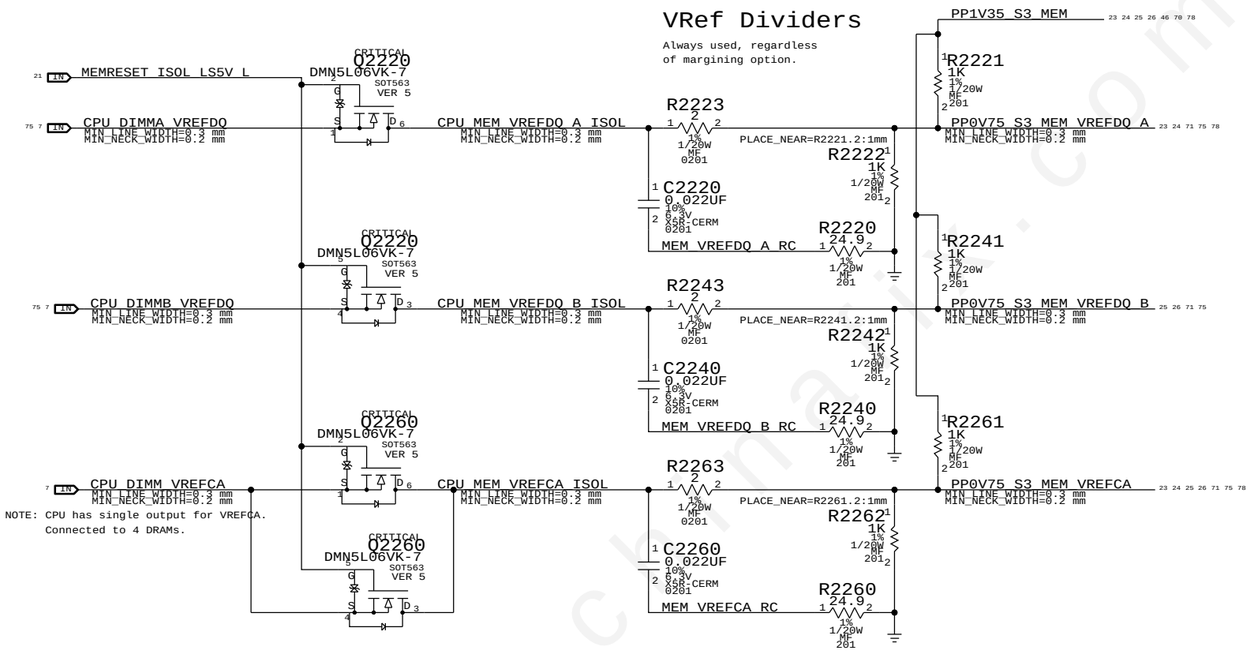
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step



NOTE: CPU has single output for VREFCA.
Connected to 4 DRAMs.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/14/2014

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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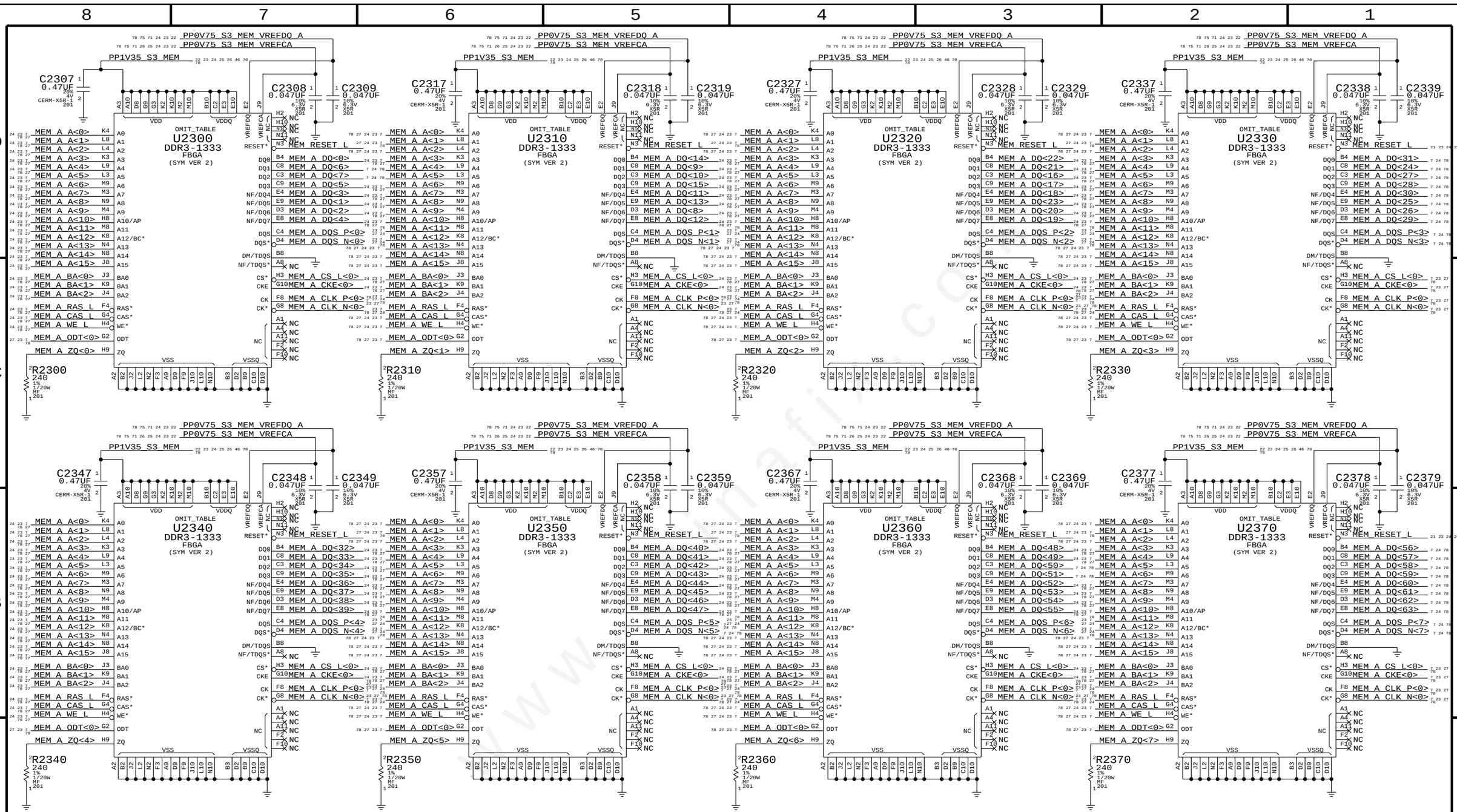

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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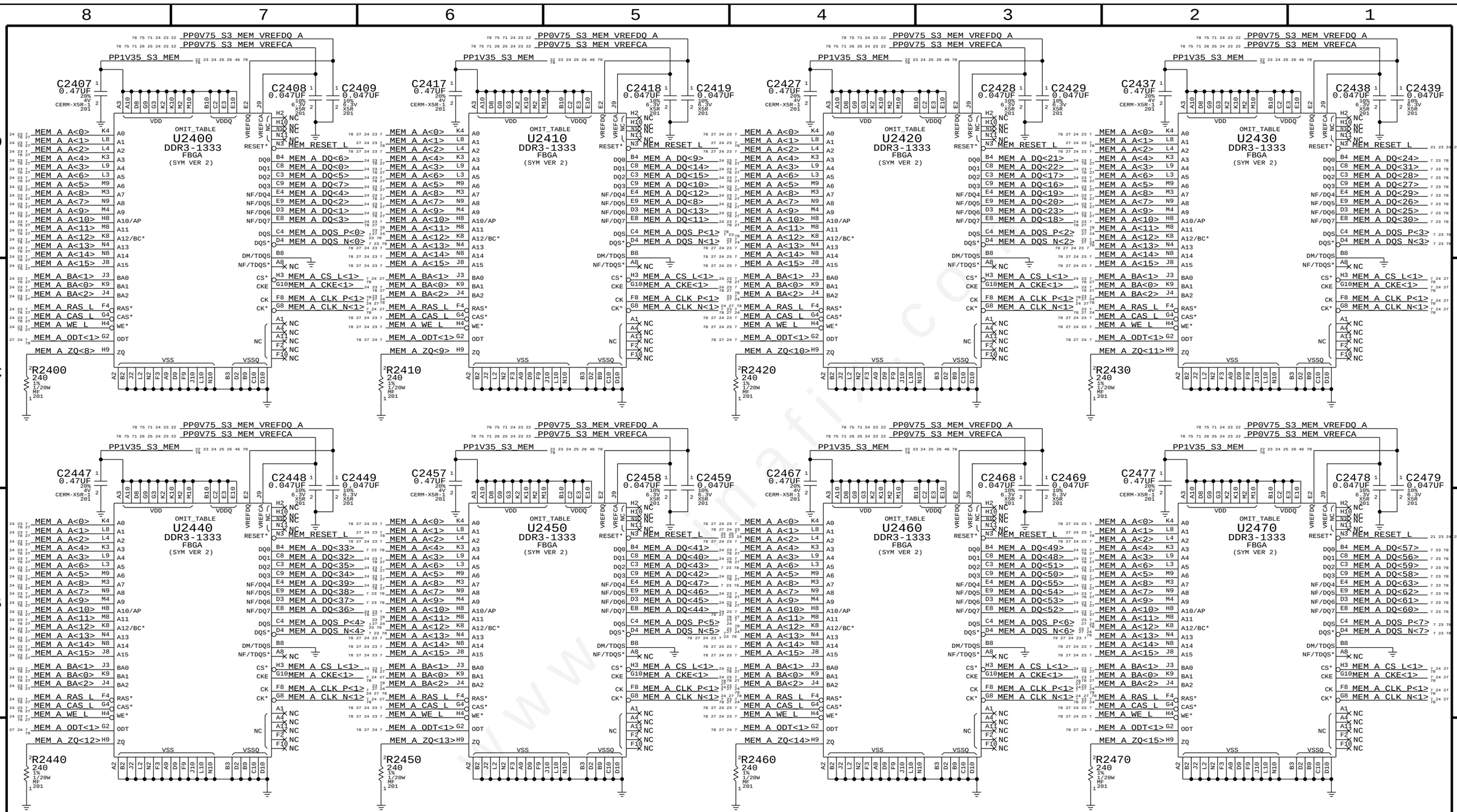

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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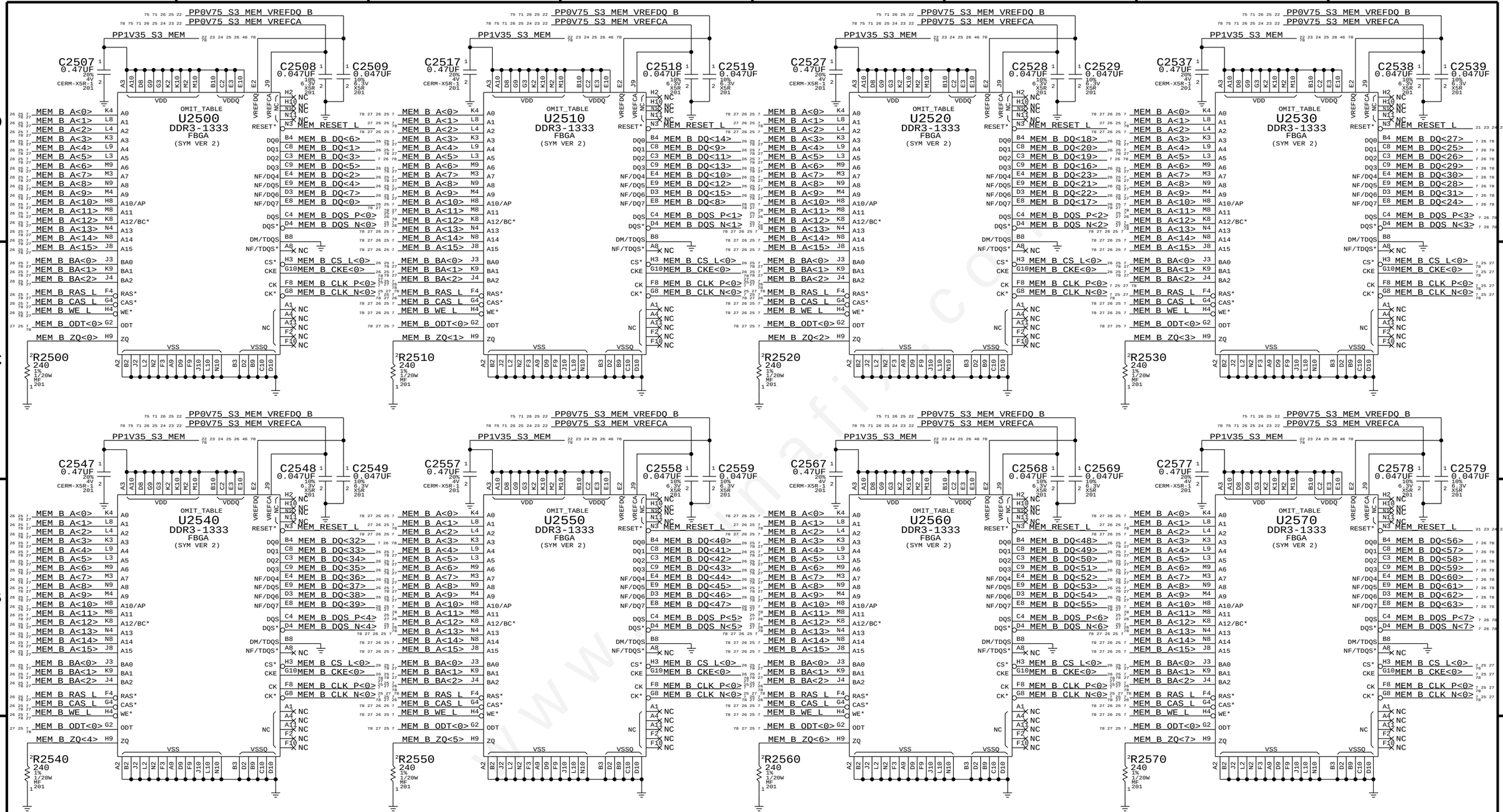
PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA
PP1V35_S3_MEM
C2507 0.47UF CERM-X5R-1 201
C2508 0.047UF 10% 6.3V X5R 201
C2509 0.047UF 10% 6.3V X5R 201
OMIT_TABLE
U2500
DDR3-1333
FBGA
(SYM VER 2)
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MEM_B_A<4>
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MEM_B_BA<2>
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MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<0>
MEM_RESET_L
MEM_B_DQ<6>
MEM_B_DQ<1>
MEM_B_DQ<3>
MEM_B_DQ<5>
MEM_B_DQ<2>
MEM_B_DQ<4>
MEM_B_DQ<7>
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MEM_B_DQS_N<0>
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MEM_B_CLK_P<0>
MEM_B_CLK_N<0>
R2500 240 1% 1/20W MF 201
C2517 0.47UF CERM-X5R-1 201
C2518 0.047UF 10% 6.3V X5R 201
C2519 0.047UF 10% 6.3V X5R 201
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DDR3-1333
FBGA
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C2527 0.47UF CERM-X5R-1 201
C2528 0.047UF 10% 6.3V X5R 201
C2529 0.047UF 10% 6.3V X5R 201
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C2538 0.047UF 10% 6.3V X5R 201
C2539 0.047UF 10% 6.3V X5R 201
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DDR3-1333
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C2549 0.047UF 10% 6.3V X5R 201
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C2559 0.047UF 10% 6.3V X5R 201
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MEM_B_CLK_N<0>
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C2568 0.047UF 10% 6.3V X5R 201
C2569 0.047UF 10% 6.3V X5R 201
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SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
C2500 2.2UF
C2501 2.2UF
C2510 2.2UF
C2511 2.2UF
C2520 2.2UF
C2521 2.2UF
C2530 2.2UF
C2531 2.2UF
C2503 0.1UF
C2504 0.1UF
C2505 0.1UF
C2513 0.1UF
C2514 0.1UF
C2515 0.1UF
C2523 0.1UF
C2524 0.1UF
C2525 0.1UF
C2533 0.1UF
C2534 0.1UF
C2535 0.1UF
C2540 2.2UF
C2541 2.2UF
C2550 2.2UF
C2551 2.2UF
C2560 2.2UF
C2561 2.2UF
C2570 2.2UF
C2571 2.2UF
C2543 0.1UF
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C2553 0.1UF
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C2564 0.1UF
C2565 0.1UF
C2573 0.1UF
C2574 0.1UF
C2575 0.1UF
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
PAGE TITLE
DDR3 SDRAM Bank B (1 OF 2)
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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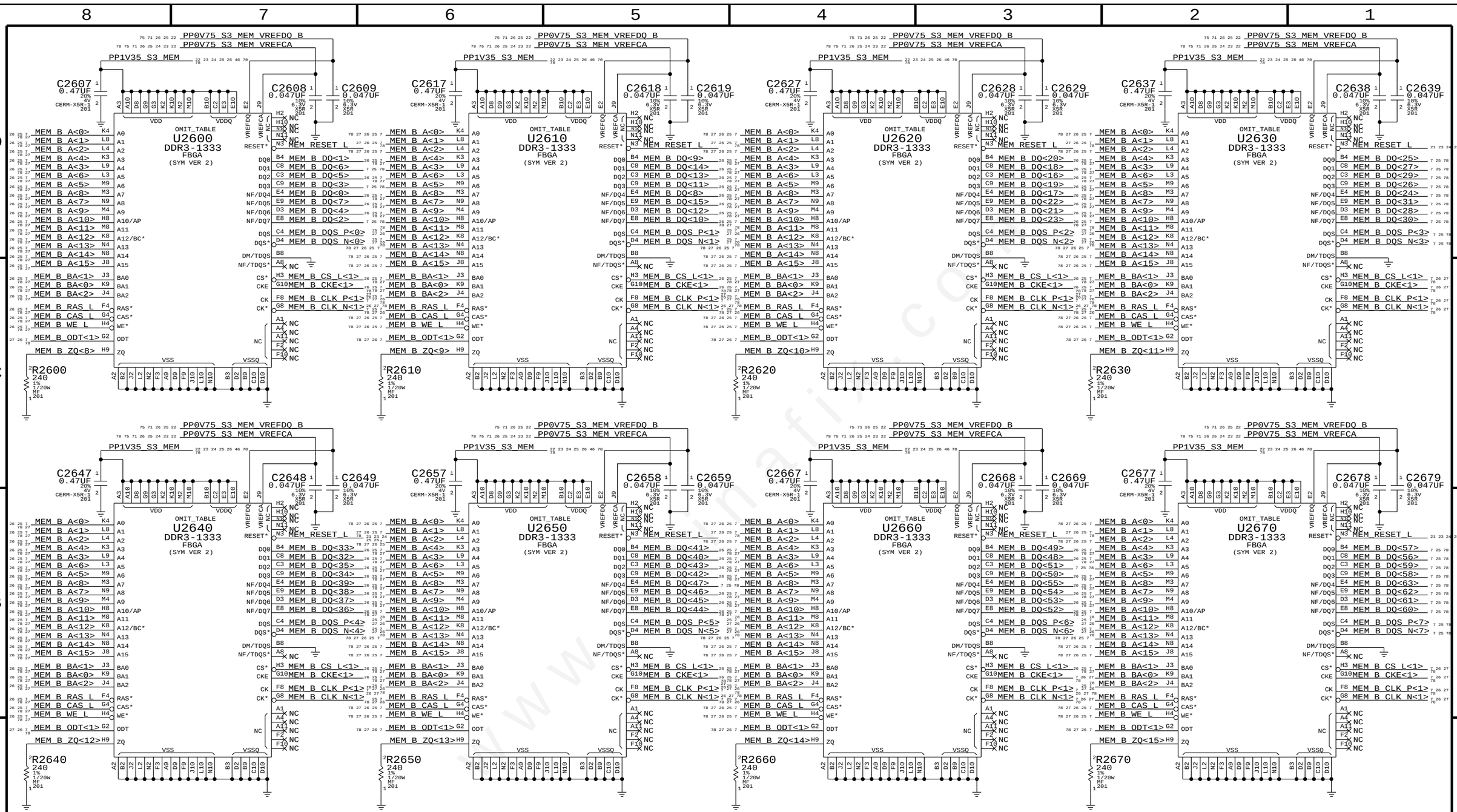

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PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

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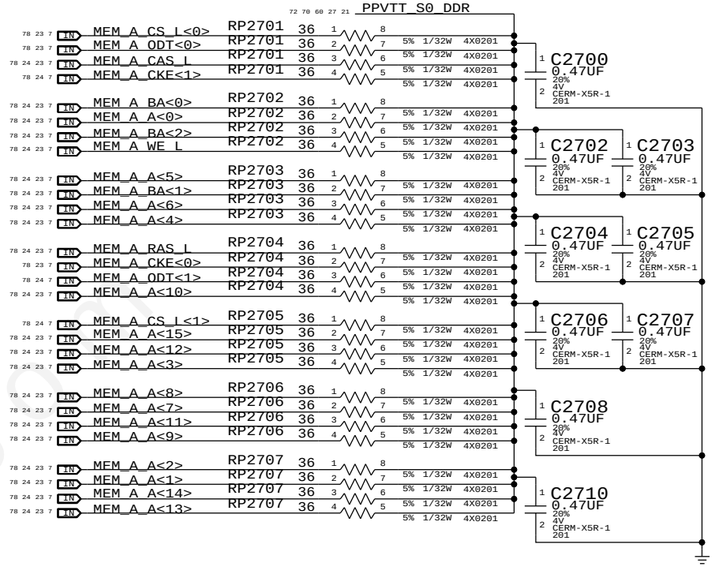
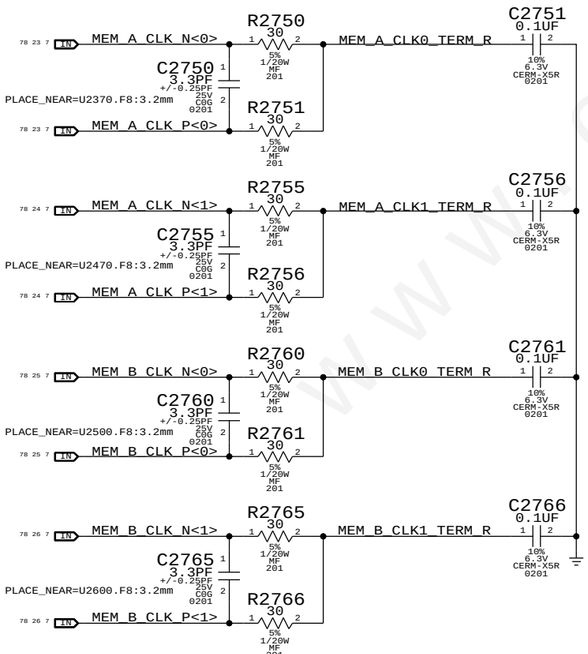
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE: DDR3 Termination	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
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OMIT_TABLE

U2800
FALCON RIDGE
FCBGA
SYM 1 OF 2
CRITICAL

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9
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PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19

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PETN_2		PCIE_TBT_D2R_N<2>
PERP_3	AD17	PCIE_TBT_D2R_C_P<3>
PERN_3	AD19	PCIE_TBT_D2R_C_N<3>
PETP_3		PCIE_TBT_D2R_P<3>
PETN_3		PCIE_TBT_D2R_N<3>

C2840–C2847 0.1UF each: PCIE_TBT_D2R_P/N<0:3> OUT

MISC

PERST_OD_N	P5	TBT_PCIE_RESET_L
PWR_ON_POC_RST_N	R4	TBT_PWR_ON_POC_RST_L
MONDC0	AD23	TP_TBT_MONDC0
MONDC1	AC24	TP_TBT_MONDC1
MONOBSP	W18	TBT_MONOBSP
MONOBSN	W16	TBT_MONOBSN
THERMDA	AB7	TBT_THERMDP
EE_DI	AA2	TBT_SPI_MOSI
EE_DO	Y3	TBT_SPI_MISO
EE_CS_N	T5	TBT_SPI_CS_L
EE_CLK	U8	TBT_SPI_CLK
TDI	W2	JTAG_TBT_TDI
TMS	AB1	JTAG_TBT_TMS
TCK	AA6	JTAG_TBT_TCK
TDO	U6	JTAG_TBT_TDO
TEST_EN	R6	TBT_TEST_EN
TEST_PWR_GOOD	W8	TBT_TEST_PWR_GOOD

DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Use AA8 GND ball for THERM_DN

RSENSE	U20	TBT_RSENSE
RBIAS	W20	TBT_RBIAS
RSVD_GND	AD1, L8	
GPIO_16/DEVICE_PCIE_RST_N	W6	TP_TBT_PCIE_RESET0_L
GPIO_17	AB3	TBT_DFT_STRAP_1
GPIO_18	AD3	TBT_ROM_SECURITY_XOR
GPIO_19	V1	TBT_DFT_STRAP_3
PCIE_CLKREQ_OD_N	V3	TBT_CLKREQ_L
REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N
XTAL_25_IN	AA24	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	AB23	NC_TBT_XTAL25OUT
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT

R2855 1K 1% 1/20W MF 201 (RBIAS)

Used for straps in host mode

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?

R2867 NO STUFF 10K 5% 1/20W MF 201 (PP3V3_TBTLC)
R2861 10K, R2862 10K, R2863 10K 5% 1/20W MF 201 (PP3V3_TBTLC)

Divides 3.3V to 1.8V
R2895 806 1% 1/20W MF 201 (SYSCLK_CLK25M_TBT_R)

DISPLAY PORT

DPSRC_3_P	A14	NC_DP_TBTSRC_ML_CP<3>
DPSRC_3_N	B15	NC_DP_TBTSRC_ML_CN<3>
DPSRC_2_P	A12	NC_DP_TBTSRC_ML_CP<2>
DPSRC_2_N	B13	NC_DP_TBTSRC_ML_CN<2>
DPSRC_1_P	A10	NC_DP_TBTSRC_ML_CP<1>
DPSRC_1_N	B11	NC_DP_TBTSRC_ML_CN<1>
DPSRC_0_P	A8	NC_DP_TBTSRC_ML_CP<0>
DPSRC_0_N	B9	NC_DP_TBTSRC_ML_CN<0>
DPSRC_AUX_P	J4	NC_DP_TBTSRC_AUXCH_CP
DPSRC_AUX_N	J2	NC_DP_TBTSRC_AUXCH_CN
DPSRC_HPD_OD	AC2	DP_TBTSRC_HPD

R2899 NO STUFF 10K 5% 1/20W MF 201
R2896 1K 5% 1/20W MF 201

PP3V3_TBTLC
R2878 100K, R2879 100K 5% 1/20W MF 201

PP3V3_S4_TBT
R2881 100K, R2880 100K, R2882 100K 5% 1/20W MF 201

R2884 100K, R2885 10K, R2886 NO STUFF 10K 5% 1/20W MF 201

R2832 100K, R2883 100K, R2888 10K, R2887 10K 5% 1/20W MF 201

PORTS

GPIO_2/TMU_CLK_IN/AC_PRESENT	U2	TBT_GPIO2
GPIO_3/FORCE_PWR	L6	TBT_PWR_EN
GPIO_4/WAKE_OD_N	H5	SMC_PME_S4_DARK_L
GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD	Y7	TBT_CIO_PLUG_EVENT_L
GPIO_6_OD/CIO_SDA_OD	Y1	HDMITBTMUX_SEL_TBT
GPIO_7_OD/CIO_SCL_OD	T7	TBT_GPIO7
GPIO_8/EN_CIO_PWR_N_OD	V7	TBT_EN_CIO_PWR_L
GPIO_9/SX_CTRL_OD*	M7	TBT_BATLOW_L
GPIO_14	T1	TBTDP_AUXIO_EN
GPIO_15	T3	TBT_DDC_XBAR_EN_L
PA_CIO0_TX_P/DPSRC_0_P		PB_CIO2_TX_P/DPSRC_0_P R24 TBT_B_R2D_C_P<0>
PA_CIO0_TX_N/DPSRC_0_N		PB_CIO2_TX_N/DPSRC_0_N N24 TBT_B_R2D_C_N<0>
PA_CIO0_RX_P		PB_CIO2_RX_P R22 TBT_B_D2R_P<0>
PA_CIO0_RX_N		PB_CIO2_RX_N N22 TBT_B_D2R_N<0>
PA_CONFIG1/CIO_0_LSEO		PB_CONFIG1/CIO_2_LSEO D3 TBT_B_CONFIG1_BUF
PA_CONFIG2/CIO_0_LSOE		PB_CONFIG2/CIO_2_LSOE M1 TBT_B_CONFIG2_RC
PA_CIO1_TX_P/DPSRC_2_P		PB_CIO3_TX_P/DPSRC_2_P W24 TBT_B_R2D_C_P<1>
PA_CIO1_TX_N/DPSRC_2_N		PB_CIO3_TX_N/DPSRC_2_N U24 TBT_B_R2D_C_N<1>
PA_CIO1_RX_P		PB_CIO3_RX_P W22 TBT_B_D2R_P<1>
PA_CIO1_RX_N		PB_CIO3_RX_N U22 TBT_B_D2R_N<1>
PA_LSTX/CIO_1_LSEO		PB_LSTX/CIO_3_LSEO M5 TBT_B_LSTX
PA_LSRX/CIO_1_LSOE		PB_LSRX/CIO_3_LSOE P7 TBT_B_LSRX
PA_DPSRC_1_P		PB_DPSRC_1_P A20 DP_TBTPB_ML_C_P<1>
PA_DPSRC_1_N		PB_DPSRC_1_N B21 DP_TBTPB_ML_C_N<1>
PA_DPSRC_3_P		PB_DPSRC_3_P A22 DP_TBTPB_ML_C_P<3>
PA_DPSRC_3_N		PB_DPSRC_3_N B23 DP_TBTPB_ML_C_N<3>
PA_AUX_P		PB_AUX_P K3 DP_TBTPB_AUXCH_C_P
PA_AUX_N		PB_AUX_N K1 DP_TBTPB_AUXCH_C_N
PA_DPSRC_HPD		PB_DPSRC_HPD N6 DP_TBTPB_HPD
GPIO_0/PA_HV_EN/BYP0		GPIO_1/PB_HV_EN/BYP0 F1 TBT_B_HV_EN
GPIO_10/PA_CIO_SEL/BYP1		GPIO_11/PB_CIO_SEL/BYP1 R2 TBT_B_CIO_SEL
GPIO_12/PA_DP_PWRDN/BYP2		GPIO_13/PB_DP_PWRDN/BYP2 F3 TBT_B_DP_PWRDN

TBT_EN_CIO_PWR_L, TBT_DDC_XBAR_EN_L, HDMITBTMUX_SEL_TBT, TBTDP_AUXIO_EN, DP_TBTSRC_HPD, TBT_BATLOW_L, TBT_A_DP_PWRDN, TBT_B_DP_PWRDN, TBT_A_HV_EN, TBT_B_HV_EN

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

R2890 3.3K, R2891 3.3K, C2890 1UF 16V 6-CSM 2 402, R2892 3.3K, R2893 3.3K 5% 1/20W MF 201 (BYPASS=U2890::2mm)

U2890 4MBIT W25X40CLXIG USON
CRITICAL OMIT_TABLE
VCC
(TBT_SPI_MOSI) DI/IO0
(TBT_SPI_CLK) CLK
(TBT_SPI_CS_L) CS*
TBTROM_WP_L WP*
TBTROM_HOLD_L HOLD*
DO/IO1 (TBT_SPI_MISO)
GND THRM_PAD

R2829 10K 5% 1/20W MF 201
R2825 100 5% 1/20W MF 201
OMIT R2815 NOSTUFF 0201

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N

DPSNK0_3_P	E14	DP_TBTSNK0_ML_P<3>
DPSNK0_3_N	D13	DP_TBTSNK0_ML_N<3>
DPSNK0_2_P	E16	DP_TBTSNK0_ML_P<2>
DPSNK0_2_N	D15	DP_TBTSNK0_ML_N<2>
DPSNK0_1_P	E18	DP_TBTSNK0_ML_P<1>
DPSNK0_1_N	D17	DP_TBTSNK0_ML_N<1>
DPSNK0_0_P	E20	DP_TBTSNK0_ML_P<0>
DPSNK0_0_N	D19	DP_TBTSNK0_ML_N<0>
DPSNK0_AUX_P	G4	DP_TBTSNK0_AUXCH_P
DPSNK0_AUX_N	G2	DP_TBTSNK0_AUXCH_N
DPSNK0_HPD	AB5	DP_TBTSNK0_HPD

R2830 100K 5% 1/20W MF 201

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N

DPSNK1_3_P	E6	DP_TBTSNK1_ML_P<3>
DPSNK1_3_N	D5	DP_TBTSNK1_ML_N<3>
DPSNK1_2_P	E8	DP_TBTSNK1_ML_P<2>
DPSNK1_2_N	D7	DP_TBTSNK1_ML_N<2>
DPSNK1_1_P	E10	DP_TBTSNK1_ML_P<1>
DPSNK1_1_N	D9	DP_TBTSNK1_ML_N<1>
DPSNK1_0_P	E12	DP_TBTSNK1_ML_P<0>
DPSNK1_0_N	D11	DP_TBTSNK1_ML_N<0>
DPSNK1_AUX_P	H3	DP_TBTSNK1_AUXCH_P
DPSNK1_AUX_N	H1	DP_TBTSNK1_AUXCH_N
DPSNK1_HPD	U4	DP_TBTSNK1_HPD

R2831 100K 5% 1/20W MF 201

PA_CIO0_TX_P/DPSRC_0_P	G24	TBT_A_R2D_C_P<0>
PA_CIO0_TX_N/DPSRC_0_N	E24	TBT_A_R2D_C_N<0>
PA_CIO0_RX_P	G22	TBT_A_D2R_P<0>
PA_CIO0_RX_N	E22	TBT_A_D2R_N<0>
PA_CONFIG1/CIO_0_LSEO	P1	TBT_A_CONFIG1_BUF
PA_CONFIG2/CIO_0_LSOE	K5	TBT_A_CONFIG2_RC
PA_CIO1_TX_P/DPSRC_2_P	L24	TBT_A_R2D_C_P<1>
PA_CIO1_TX_N/DPSRC_2_N	J24	TBT_A_R2D_C_N<1>
PA_CIO1_RX_P	L22	TBT_A_D2R_P<1>
PA_CIO1_RX_N	J22	TBT_A_D2R_N<1>
PA_LSTX/CIO_1_LSEO	N8	TBT_A_LSTX
PA_LSRX/CIO_1_LSOE	J6	TBT_A_LSRX
PA_DPSRC_1_P	A16	DP_TBTPA_ML_C_P<1>
PA_DPSRC_1_N	B17	DP_TBTPA_ML_C_N<1>
PA_DPSRC_3_P	A18	DP_TBTPA_ML_C_P<3>
PA_DPSRC_3_N	B19	DP_TBTPA_ML_C_N<3>
PA_AUX_P	L4	DP_TBTPA_AUXCH_C_P
PA_AUX_N	L2	DP_TBTPA_AUXCH_C_N
PA_DPSRC_HPD	M3	DP_TBTPA_HPD
GPIO_0/PA_HV_EN/BYP0	R8	TBT_A_HV_EN
GPIO_10/PA_CIO_SEL/BYP1	N2	TBT_A_CIO_SEL
GPIO_12/PA_DP_PWRDN/BYP2	P3	TBT_A_DP_PWRDN

SYNC_MASTER=T29_RR	SYNC_DATE=01/14/2013
PAGE TITLE	Thunderbolt Host (1 of 2)
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	REVISION <E4LABEL>
	BRANCH <BRANCH>
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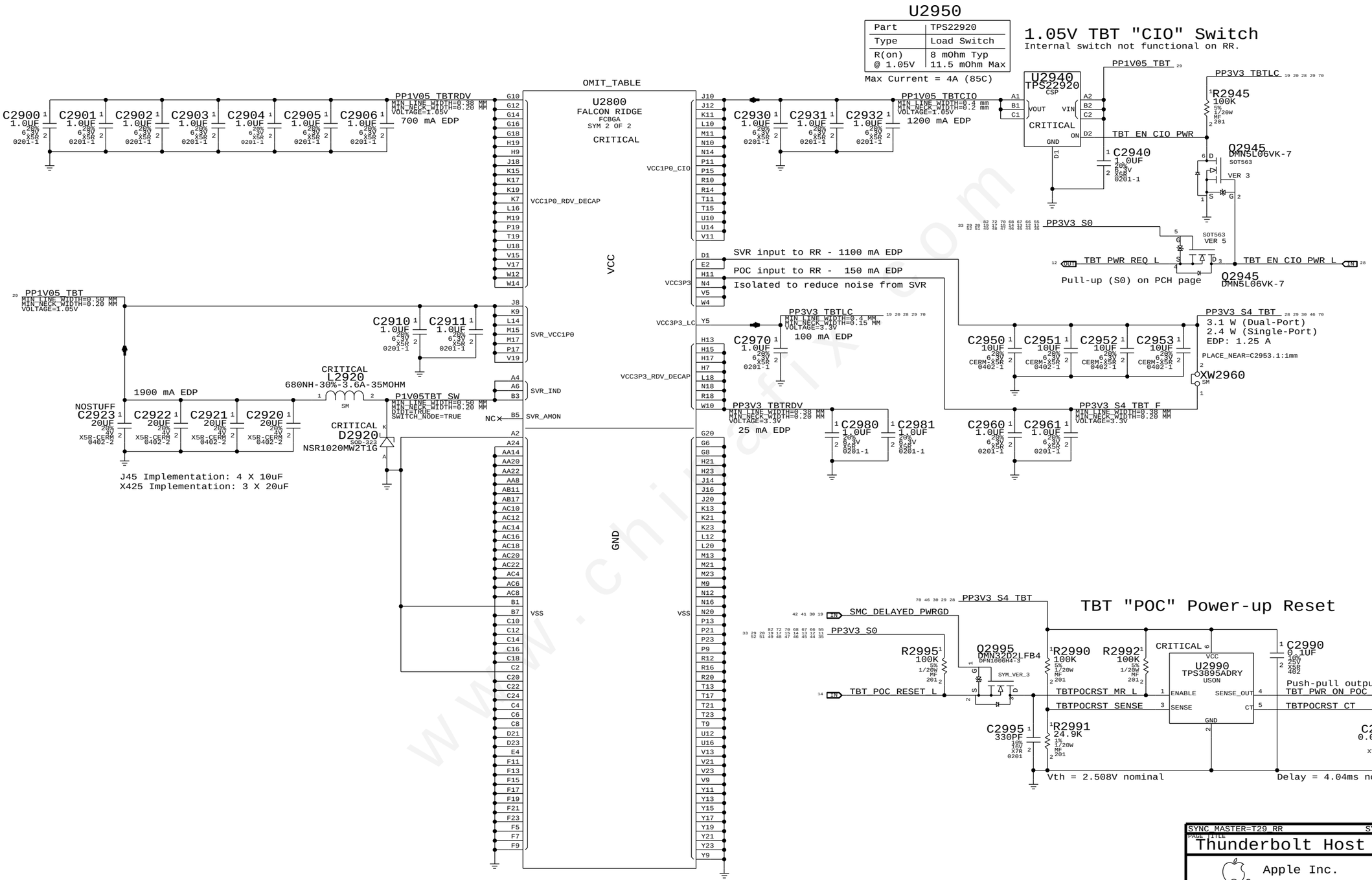
U2950
Part | TPS22920
Type | Load Switch
R(on) @ 1.05V | 8 mOhm Typ 11.5 mOhm Max
Max Current = 4A (85C)
1.05V TBT "CIO" Switch
Internal switch not functional on RR.
U2940 TPS22920 CSP
CRITICAL
PP1V05_TBT
PP3V3_TBTLC
R2945 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
Q2945 DMN5L06VK-7 SOT563 VER 3
C2940 1.0UF 20% 6.3V X5R 0201-1
PP3V3_S0
SOT563 VER 5
TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L
Q2945 DMN5L06VK-7
Pull-up (S0) on PCH page
OMIT_TABLE
U2800 FALCON RIDGE FCBGA SYM 2 OF 2
CRITICAL
VCC
VSS
GND
PP1V05_TBTRDV
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.05V
700 mA EDP
C2900 C2901 C2902 C2903 C2904 C2905 C2906 1.0UF 20% 6.3V X5R 0201-1
VCC1P0_RDV_DECAP
PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
1200 mA EDP
C2930 C2931 C2932 1.0UF 20% 6.3V X5R 0201-1
VCC1P0_CIO
SVR input to RR - 1100 mA EDP
POC input to RR - 150 mA EDP
Isolated to reduce noise from SVR
VCC3P3
PP1V05_TBT
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.05V
C2910 C2911 1.0UF 20% 6.3V X5R 0201-1
SVR_VCC1P0
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=3.3V
100 mA EDP
C2970 1.0UF 20% 6.3V X5R 0201-1
VCC3P3_LC
VCC3P3_RDV_DECAP
PP3V3_S4_TBT
3.1 W (Dual-Port)
2.4 W (Single-Port)
EDP: 1.25 A
PLACE_NEAR=C2953.1:1mm
C2950 C2951 C2952 C2953 10UF 20% 6.3V CERM-X5R 0402-1
XW2960 SM
NOSTUFF
C2923 20UF 20% 6V X5R-CERM 0402-2
1900 mA EDP
C2922 C2921 C2920 20UF 20% 6V X5R-CERM 0402-2
J45 Implementation: 4 X 10uF
X425 Implementation: 3 X 20uF
CRITICAL
L2920
680NH-30%-3.6A-35MOHM
SM
P1V05TBT_SW
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
DIDT=TRUE
SWITCH_NODE=TRUE
SVR_IND
SVR_AMON
NCX
CRITICAL
D2920
SOD-323
NSR1020MW2T1G
PP3V3_TBTRDV
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
25 mA EDP
C2980 C2981 1.0UF 20% 6.3V X5R 0201-1
PP3V3_S4_TBT_F
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
C2960 C2961 1.0UF 20% 6.3V X5R 0201-1
TBT "POC" Power-up Reset
PP3V3_S4_TBT
SMC_DELAYED_PWRGD
PP3V3_S0
R2995 100K 5% 1/20W MF 201
Q2995 DMN32D2LFB4 DFN1006H4-3
SYM_VER_3
TBT_POC_RESET_L
R2990 100K 5% 1/20W MF 201
R2992 100K 5% 1/20W MF 201
TBTPOCRST_MR_L
TBTPOCRST_SENSE
CRITICAL
U2990 TPS3895ADRY USON
ENABLE
SENSE
SENSE_OUT
CT
GND
C2990 0.1UF 10% 16V X5R 402
Push-pull output
TBT_PWR_ON_POC_RST_L
TBTPOCRST_CT
C2995 330PF 10% 16V X7R 0201
R2991 24.9K 1% 1/20W MF 201
C2991 0.001UF 10% 50V X7R-CERM 0402
Vth = 2.508V nominal
Delay = 4.04ms nominal
EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).
SYNC_MASTER=T29_RR
SYNC_DATE=01/14/2013
PAGE TITLE
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Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/16W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

Q3005 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
TBT_A_HV_EN
Second FET needed for dual-port designs.

CRITICAL
Q3080 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here,
add property on another page.

R3091 200K 1% 1/10W MF-LF 402 <R1>
R3092 73.2K 1% 1/10W MF-LF 402 <R2>

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V CERM 0402
C3092 2.2UF 20% 10V X5R-CERM 402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3093 49.9K 1% 1/10W MF-LF 402
R3094 26.7K 1% 1/10W MF-LF 402
C3094 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095 3.3UH-6.5A PIMB063T-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090 LT3957 QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

SGND shorted to GND inside package, no XW necessary.

TBTBST_SNS1
R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5
TBTBST_SNS2
R3097 10 5% 1/16W MF-LF 402

NOTE: Change R3097 to XW3095 at PVT

TBTBST_VSNS
C3088 10PF 5% 50V CERM 0402
R3095 137K 1% 1/10W MF-LF 402 <Ra>
TBTBST_FBX
NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/10W MF-LF 402 <Rb>

Vout = 1.6V * (1 + Ra / Rb)

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

PP15V_TBT
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz

C3096 10UF 20% 25V X5R-CERM 0603
NO STUFF
C3097 10UF 10% 25V X7R-CERM 1206
C3099 0.001UF 10% 50V X7R-CERM 0402
C3098 10UF 20% 25V X5R-CERM 0603

PLACE_SIDE=BOTTOM
PLACE_SIDE=TOP

NOTE: MIRROR C3096 and C3098

Q3088 DMN5L06VK-7 SOT563 VER 3
R3088 330K 5% 1/10W MF-LF 402
Max Vgs: 10V
TBTBST_SHDN_DIV
R3087 330K 5% 1/10W MF-LF 402
Q3088 DMN5L06VK-7 SOT563 VER 3
SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: Thunderbolt Mobile Support

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT 15.75V Max
CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 603
C3281 0.1UF 10% 16V X5R-CERM 0201
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 25V X5R 402
CRITICAL U3210 CD3211A1RGP QFN
V3P3 V3P3OUT VHV OUT ENHVU FAULTZ EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTAPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
PP3V3RHV_S4_TBTAPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_R_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V R3210 22.6K 1% 1/20W MF 201
TBTHV:P15V R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
12V: See below
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
TBTHV:P15V R3213 22.6K 1% 1/20W MF 201 <RHVS3>
TBTHV:P15V R3214 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector A

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3220 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
GND_VOID=TRUE (Both C's)
TBT_A_D2R_N<1> C3277 0.47UF 20% 4V_201 CERM-X5R-1
TBT_A_D2R_P<1> C3276 0.47UF 20% 4V_201 CERM-X5R-1
DP_TBTPA_AUXCH_C_N C3230 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_AUXCH_C_P C3231 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_ML_C_P<1> C3232 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_N<1> C3233 0.22UF 20% 6.3V X5R 0201
TBT_A_D2R_C_N<1> TBT_A_D2R_C_P<1> DP_TBTPA_AUXCH_N DP_TBTPA_AUXCH_P DP_TBTPA_DDC_DATA DP_TBTPA_DDC_CLK TBT_A_CONFIG1_BUF DP_TBTPA_ML_P<1> DP_TBTPA_ML_N<1> TBT_A_LSTX TBT_A_LSRX DP_TBTPA_HPD
TB- TB+ AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX (IPU) LSRX (IPD) HPDOUT
TB_ENA AUXIO_EN DP_PD (IPU)AUXIO- (IPD)AUXIO+ CA_DET DPML0+ DPML0- HPD
TBT_A_CIO_SEL TBTDP_AUXIO_EN TBT_A_DP_PWRDN TBT_A_D2R1_AUXDDC_N TBT_A_D2R1_AUXDDC_P TBT_A_CONFIG1_RC DP_A_LSX_ML_P<1> DP_A_LSX_ML_N<1> TBT_A_HPD
GND_THMPAD
TBT: RX_1
TBT: LSX_A_R2P/P2R (P/N)

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C3200 0.01UF 10% 50V X7R-CERM 0402
R3201 12 5% 1/20W MF 201
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V
TBTACONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
TBTACONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
GND_VOID=TRUE C3205 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
GND_VOID=TRUE C3206 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
CRITICAL J3200 MDP-J44 F-RT-TH
SHIELD PINS S16 S15 S14 S13 S12
PORT B
SHIELD PINS S24 S22 S21 S20 S19 S18 S17
514-0876
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
GND_VOID=TRUE (Both C's)
TBT_A_D2R_P<0> C3274 0.47UF 20% 4V_201 CERM-X5R-1
TBT_A_D2R_N<0> C3275 0.47UF 20% 4V_201 CERM-X5R-1
R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
DP_TBTPA_ML_C_P<3> C3278 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_N<3> C3279 0.22UF 20% 6.3V X5R 0201
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
TBT_A_D2R1_AUXDDC_P TBT_A_D2R1_AUXDDC_N
TBT_A_HPD TBT_A_CONFIG1_RC TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R 0201
C3295 330PF 10% 16V X7R 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 16V X5R-CERM 0201
TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
DP Dir TBT Dir
TBT: TX_0
TBT: TX_1
GND_VOID=TRUE (Both C's)
TBT_A_R2D_P<0> C3270 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_N<0> C3271 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
TBT_A_R2D_P<1> C3272 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_N<1> C3273 0.22UF 20% 6.3V X5R 0201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT 15.75V Max
CRITICAL U3310 CD3211A1RGP QFN
S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_R_L
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V
12V: See below
R3310 22.6K 1% 1/20W MF 201
R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201 <RV3P3>
R3313 22.6K 1% 1/20W MF 201 <RHVS3>
R3314 22.6K 1% 1/20W MF 201 <RHVS0>
ILIM = 40000 / RISET
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

PP3V3_S4_TBTBPWR
PP3V3R3V_S4_TBTBPWR

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

CRITICAL L3300 FERR-120-OHM-3A 0603
PP3V3R3V_S4_TBTBPWR_F
C3300 0.01UF 10% 50V X7R-CERM 0402
C3301 0.01UF 10% 50V X7R-CERM 0402
R3301 12 5% 1/20W MF 201
TBTCONN_20_RC
TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1

CRITICAL J3200 MDP-J44 F-RT-TH
SHIELD PINS
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
PORT A
514-0876

TBT_B_D2R_P<0> TBT_B_D2R_N<0> C3374 0.47UF 20% 4V_201 CERM-X5R-1
TBT_B_D2R_P<1> TBT_B_D2R_N<1> C3375 0.47UF 20% 4V_201 CERM-X5R-1
TBT_B_D2R_C_P<0> TBT_B_D2R_C_N<0>
TBT_B_D2R_C_P<1> TBT_B_D2R_C_N<1>
GND_VOID=TRUE (Both C's)
R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE

DP_TBTPB_ML_C_P<3> DP_TBTPB_ML_C_N<3> C3378 0.22UF 20% 6.3V X5R 0201 C3379 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_P<3> DP_TBTPB_ML_C_N<3>
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201

TBT_B_D2R1_AUXDDC_P TBT_B_D2R1_AUXDDC_N

TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R 0201
C3395 330PF 10% 16V X7R 0201
R3341 100K 5% 1/20W MF 201
C3302 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
SIGNAL_MODEL=TBT_MUX
CRITICAL U3320 CBTL05024 HVQFN24-COMBO

TBT_B_D2R_C_N<1> TBT_B_D2R_C_P<1> C3377 0.47UF 20% 4V_201 CERM-X5R-1 C3376 0.47UF 20% 4V_201 CERM-X5R-1
DP_TBTPB_AUXCH_C_N DP_TBTPB_AUXCH_C_P C3330 0.1UF 10% 16V X5R-CERM 0201 C3331 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPB_DDC_DATA DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1> DP_TBTPB_ML_C_N<1> C3332 0.22UF 20% 6.3V X5R 0201 C3333 0.22UF 20% 6.3V X5R 0201
TBT_B_LSTX TBT_B_LSRX
DP_TBTPB_HPD

TB- TB+ AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX (IPU) LSRX (IPD) HPDOUT
TB_ENA AUXIO_EN DP_PD (IPU)AUXIO- (IPD)AUXIO+ CA_DET DPMLO+ DPMLO- HPD
TBT_B_CIO_SEL TBTDP_AUXIO_EN TBT_B_DP_PWRDN TBT_B_D2R1_AUXDDC_N TBT_B_D2R1_AUXDDC_P
TBT: RX_1
TBT_B_CONFIG1_RC
DP_B_LSX_ML_P<1> DP_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
GND_THMPAD

TBTBCONN_1_C (0-18.9V) C3305 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C (0-18.9V) C3306 0.01UF 10% 25V X5R-CERM 0201
DP_Dir TBT_Dir
TBT_B_R2D_P<0> TBT_B_R2D_N<0>
TBT: TX_0
TBT_B_R2D_P<1> TBT_B_R2D_N<1>
TBT: TX_1
DP_B_LSX_ML_P<1> DP_B_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

GND_VOID=TRUE (Both C's)
C3370 0.22UF 20% 6.3V X5R 0201 C3371 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<0> TBT_B_R2D_C_N<0>
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
C3372 0.22UF 20% 6.3V X5R 0201 C3373 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<1> TBT_B_R2D_C_N<1>
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

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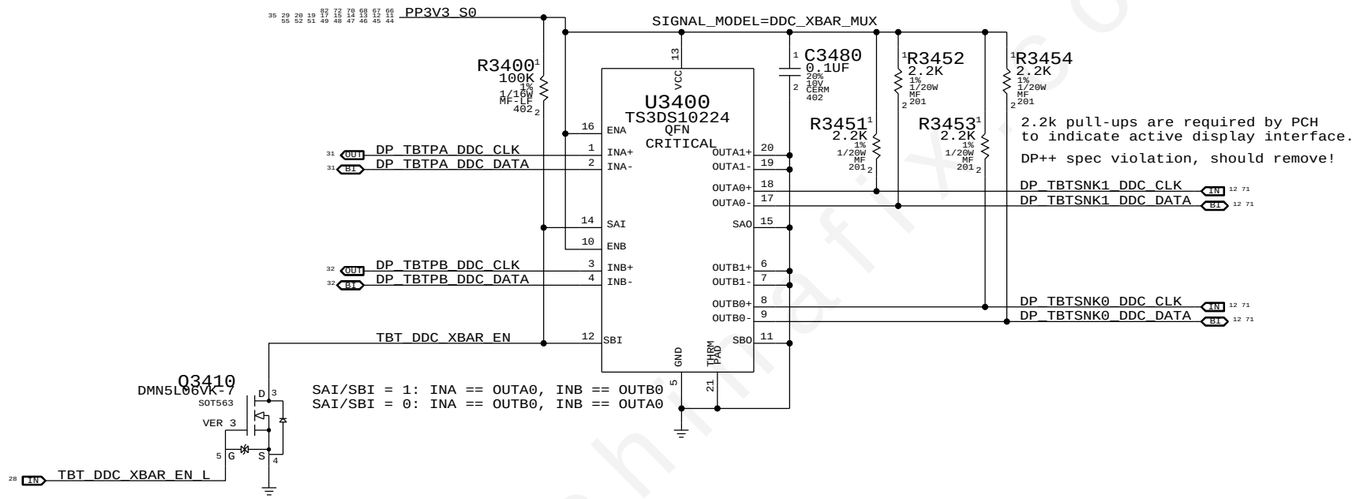
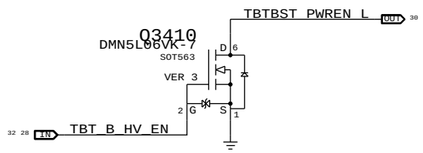
DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



SYNC_MASTER=J15_REFERENCE SYNC_DATE=11/16/2012

PAGE TITLE: DDC Crossbar

Apple Inc.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		

AIRPORT

OMIT_TABLE
L3570 0.6NH+/-0.1NH-0.85A 0201
C3531 0.1UF 10% 16V 0402 X7R-CERM PLACE_NEAR=J3501.5:2.54MM
PCIE_AP_R2D_PI_P
NOSTUFF C3570 0.1UF 10% 16V X5R-CERM 0201
NOSTUFF C3571 0.1UF 10% 16V X5R-CERM 0201
L3571 0.6NH+/-0.1NH-0.85A 0201
C3530 0.1UF 10% 16V 0402 X7R-CERM PLACE_NEAR=J3501.4:2.54MM
PCIE_AP_R2D_C_P
PCIE_AP_R2D_PI_N
WIFI_EVENT_L
NOSTUFF C3572 0.1UF 10% 16V X5R-CERM 0201
OMIT_TABLE
NOSTUFF C3573 0.1UF 10% 16V X5R-CERM 0201
OMIT_TABLE
L3573 0.6NH+/-0.1NH-0.85A 0201
PCIE_AP_D2R_P
PCIE_AP_R2D_P
PCIE_AP_R2D_N
NOSTUFF C3574 0.1UF 10% 16V X5R-CERM 0201
NOSTUFF C3575 0.1UF 10% 16V X5R-CERM 0201
L3574 0.6NH+/-0.1NH-0.85A 0201
PCIE_AP_D2R_N
NOSTUFF C3576 0.1UF 10% 16V X5R-CERM 0201
OMIT_TABLE
NOSTUFF C3577 0.1UF 10% 16V X5R-CERM 0201
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N
CRITICAL J3501 SSD-X29-D1 F-RT-SM 516S1016
CRITICAL L3501 90-OHM-0.1A-0.7-2GHZ TAM0605 SYM_VER_1 PLACE_NEAR=J3501.7:2.54MM
PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P

BLUETOOTH

PCIE_WAKE_L
PP3V3_S3RS4_BT_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
L3505 FERR-120-OHM-1.5A 0402-LF
C3532 0.01UF 10% 16V X7R-CERM 0402 PLACE_NEAR=J3501.18:2.54MM
PP3V3_S4
PP3V3_S4
C3510 0.1UF 10% 6.3V CERM-X5R 0201
NO_XNET_CONNECTION=TRUE
Q3510 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
SMC_PME_S4_WAKE_L
USB_BT_CONN_N
USB_BT_CONN_P
U3510 PI3USB102EZLE TQFN CRITICAL
NC
USB_BT_WAKEN
USB_BT_P
USB_BT_N
R3512 15K 1% 1/20W MF 201
PM_SLP_S4_L
SIGNAL_MODEL=MOJO_MUX_USBONLY

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

AP_RESET_CONN_L
AP_CLKREQ_Q_L

3.3V TI WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

155S0367
L3504 FERR-120-OHM-3A 0603
1A PEAK
PP3V3_WLAN MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
PP3V3_WLAN_F MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
C3522 0.1UF 10% 16V CERM 402 PLACE_NEAR=J3501.1:2.54MM
C3521 0.1UF 10% 16V CERM 402 PLACE_NEAR=J3501.1:2.54MM
WLAN_SW:TI
U3550 TPS22924 CSP CRITICAL
CURRENT SENSE
PP3V3_WLAN_R MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
Max Current = 2A (85C)
PP3V3_S5
PM_WLAN_EN
C3540 0.1UF 10% 16V CERM 402

3.3V SIL WLAN Switch

Part	SLG5AP1443V
Type	Load Switch
R(on) @ 2.5V	17 mOhm Typ 19 mOhm Max

WLAN_SW:SIL
U3551 SLG5AP1443V TDFN CRITICAL
PM_WLAN_CAP
C3555 4700PF 10% 16V X7R 201
PP3V3_WLAN_R

Supervisor & CLKREQ # Isolation

Delay = 130 ms +/- 20%

R3553 100K 1% 1/10W MF-LF 402
R3554 232K 1% 1/10W MF-LF 402
R3555 100K 1% 1/10W MF-LF 402
P3V3WLAN_VMON
U3540 SLG4AP041V TDFN CRITICAL
AP_RESET_L
APCLKRQ:ISOL
R3556 0 5% 1/20W MF 0201
APCLKRQ:BIDIR
R3557 1K 5% 1/20W MF 201
AP_CLKREQ_L

NOTE: Stuff non-zero value for R3557 to see which end is driving low

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE: X87 CONNECTOR

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 35 OF 118
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FOR DESENSE IMPROVEMENT

C3722 12PF 5% 50V C0G 0201 PLACE_NEAR=J3700.3:2mm
C3723 12PF 5% 50V C0G 0201 PLACE_NEAR=J3700.4:2mm
C3724 12PF 5% 50V C0G 0201 PLACE_NEAR=J3700.5:2mm

PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700 FERR-26-OHM-6A 0603

72 70 46 35 PP3V3_S0SW_SSD

C3701 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=L3700.1:1mm
C3702 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=L3700.1:1mm

PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V

514S0449
CRITICAL
J3700 SSD-GS3 F-RT-SM

NOSTUFF R3700 100K 1% 1/20W MF 201

33 29 20 82 72 70 68 67 66 55 52 51 49 48 47 46 45 44 35 PP3V3_S0

GND_VOID 1
2 SMC_OOB1_R2D_CONN_L
3 SMC_OOB1_D2R_CONN_L
4
5
6
7 PP3V3_S0
8 SSD_RESET_CONN_L
9 NC_SSD_MFG_RSVD
NO_TEST=TRUE
10
11 PCIE_SSD_R2D_N<3>
12 PCIE_SSD_R2D_P<3>
13
14 PCIE_SSD_R2D_N<2>
15 PCIE_SSD_R2D_P<2>
16
17
18 PCIE_SSD_R2D_N<1>
19 PCIE_SSD_R2D_P<1>
20
21 PCIE_SSD_R2D_N<0>
22 PCIE_SSD_R2D_P<0>
23
24 SSD_CLKREQ_CONN_L
25
26
27
28
54
55
56
57
58

53 GND_VOID
52 SMC_OOB1_R2D_CONN_L
51 SMC_OOB1_D2R_CONN_L
50 SSD_PCIE_SEL_L OUT 18
49 SSD_DEVSLP IN 20
48 SMC_PWRFAIL_WARN_L IN 41
47 SSD_PWR_FET_EN IN 35 66
46
45 TRUE PCIE_SSD_D2R_N<3> OUT 5 71 75
44 TRUE PCIE_SSD_D2R_P<3> OUT 5 71 75
43
42 TRUE PCIE_SSD_D2R_N<2> OUT 5 71 75
41 TRUE PCIE_SSD_D2R_P<2> OUT 5 71 75
40
39
38 TRUE PCIE_SSD_D2R_N<1> OUT 5 71 75
37 TRUE PCIE_SSD_D2R_P<1> OUT 5 71 75
36
35 TRUE PCIE_SSD_D2R_N<0> OUT 5 71 75
34 TRUE PCIE_SSD_D2R_P<0> OUT 5 71 75
33
32
31 PCIE_CLK100M_SSD_N IN 11 77
30 PCIE_CLK100M_SSD_P IN 11 77
29
59
60
61
62
63

Gumstick3 Connector

75 71 5 IN PCIE_SSD_R2D_C_N<3> C3710 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
75 71 5 IN PCIE_SSD_R2D_C_P<3> C3711 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
75 71 5 IN PCIE_SSD_R2D_C_N<2> C3712 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
75 71 5 IN PCIE_SSD_R2D_C_P<2> C3713 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
75 71 5 IN PCIE_SSD_R2D_C_N<1> C3714 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
75 71 5 IN PCIE_SSD_R2D_C_P<1> C3715 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
75 71 5 IN PCIE_SSD_R2D_C_N<0> C3716 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
75 71 5 IN PCIE_SSD_R2D_C_P<0> C3717 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

OOB Isolation

72 70 46 35 PP3V3_S0SW_SSD

BYPASS=U3710::5 mm
C3718 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3710 08
SMC_OOB1_R2D_L IN 41
NC

33 29 20 82 72 70 68 67 66 55 52 51 49 48 47 46 45 44 35 PP3V3_S0

BYPASS=U3711::5 mm
C3719 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3711 08
SMC_OOB1_D2R_L OUT 41
NC

R3701 100K 1% 1/20W MF 201

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD 35 46 70 72
PP3V42_G3H 19 38 39 41 42 43 44 50 56 57 65 67 70 72

R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
P3V3SSD_VMON

CRITICAL
U3740 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR* 3
EN 6
IN 7
OUT (OD) 8
THRM PAD
GND

C3740 0.1UF 10% 6.3V CERM-X5R 0201

APN 343S0511

SSD_RESET_L IN 20
SSD_PWR_FET_EN IN 35 66
SSD_CLKREQ_L OUT 11

R3742 100K 1% 1/20W MF 201

66 35 SSD_PWR_FET_EN = SSD_PWR_FET_EN 35 66
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: SSD Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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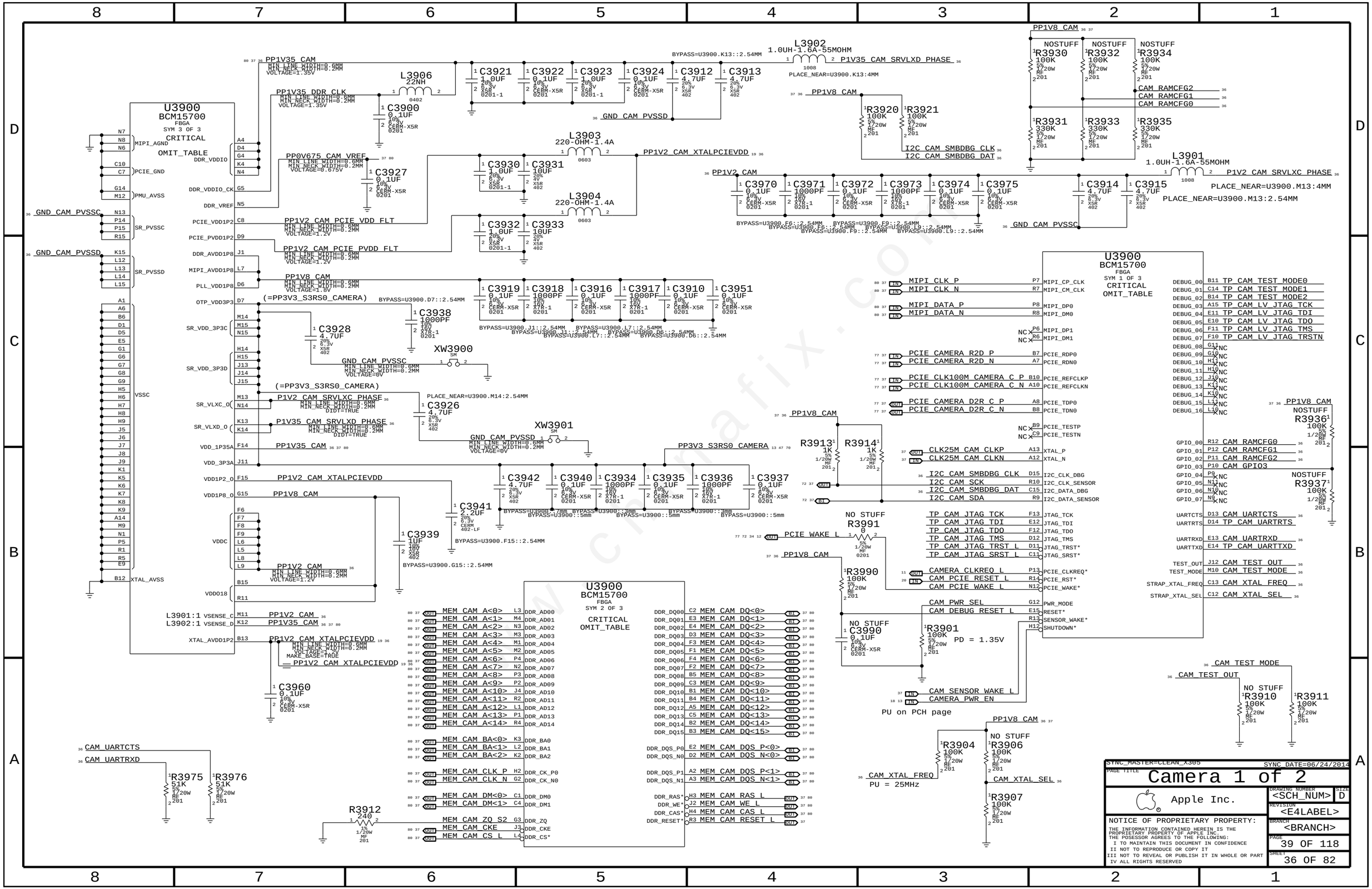
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
L3902
1.0UH-1.6A-55MOHM
L3901
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP1V35 CAM
PP1V35 DDR CLK
PP0V675 CAM VREF
PP1V2 CAM PCIE VDD FLT
PP1V2 CAM PVDD FLT
PP1V8 CAM
PP1V2 CAM XTALPCIEVDD
PP1V35 CAM SRVLXD PHASE
PP1V2 CAM SRVLXC PHASE
GND CAM PVSSD
GND CAM PVSSC
(=PP3V3_S3RS0_CAMERA)
PP3V3_S3RS0_CAMERA
XW3900
XW3901
MIPI CLK P
MIPI CLK N
MIPI DATA P
MIPI DATA N
PCIE CAMERA R2D P
PCIE CAMERA R2D N
PCIE CLK100M CAMERA C P
PCIE CLK100M CAMERA C N
PCIE CAMERA D2R C P
PCIE CAMERA D2R C N
CLK25M CAM CLKP
CLK25M CAM CLKN
I2C CAM SMBDBG CLK
I2C CAM SCK
I2C CAM SMBDBG DAT
I2C CAM SDA
TP CAM JTAG TCK
TP CAM JTAG TDI
TP CAM JTAG TDO
TP CAM JTAG TMS
TP CAM JTAG TRST L
TP CAM JTAG SRST L
CAMERA CLKREQ L
CAM PCIE RESET L
CAM PCIE WAKE L
CAM PWR SEL
CAM DEBUG RESET L
CAM SENSOR WAKE L
CAMERA PWR EN
PCIE WAKE L
PU on PCH page
PU = 1.35V
PU = 25MHz
CAM UARTCTS
CAM UARTRXD
CAM TEST MODE
CAM TEST OUT
CAM RAMCFG2
CAM RAMCFG1
CAM RAMCFG0
CAM GPIO3
CAM XTAL FREQ
CAM XTAL SEL
MEM CAM A<0>
MEM CAM A<1>
MEM CAM A<2>
MEM CAM A<3>
MEM CAM A<4>
MEM CAM A<5>
MEM CAM A<6>
MEM CAM A<7>
MEM CAM A<8>
MEM CAM A<9>
MEM CAM A<10>
MEM CAM A<11>
MEM CAM A<12>
MEM CAM A<13>
MEM CAM A<14>
MEM CAM BA<0>
MEM CAM BA<1>
MEM CAM BA<2>
MEM CAM CLK P
MEM CAM CLK N
MEM CAM DM<0>
MEM CAM DM<1>
MEM CAM ZQ S2
MEM CAM CKE
MEM CAM CS L
MEM CAM DQ<0>
MEM CAM DQS P<0>
MEM CAM DQS N<0>
MEM CAM DQS P<1>
MEM CAM DQS N<1>
MEM CAM RAS L
MEM CAM WE L
MEM CAM CAS L
MEM CAM RESET L
SYNC_MASTER=CLEAN_X305
SYNC_DATE=06/24/2014
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
39 OF 118
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36 OF 82
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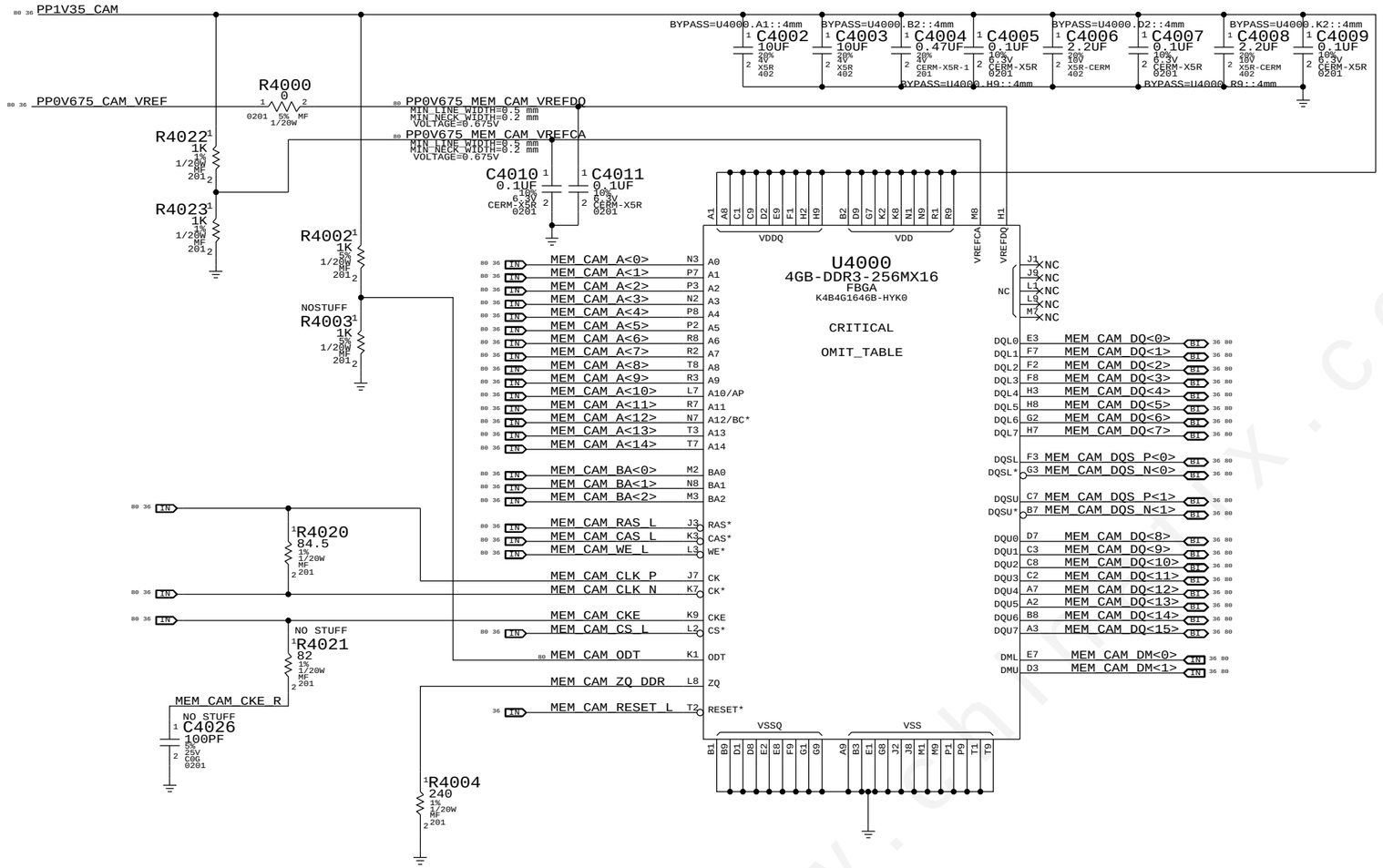

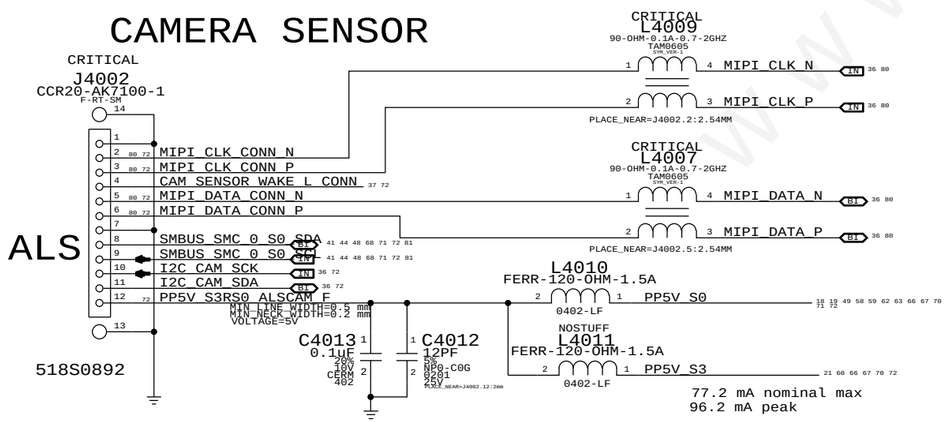

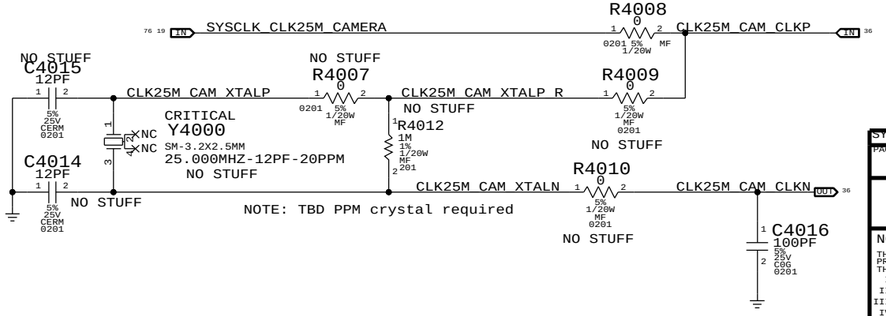

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

SYNC_MASTER=CLEAN_X305
SYNC_DATE=06/24/2014
PAGE TITLE: Camera 2 of 2
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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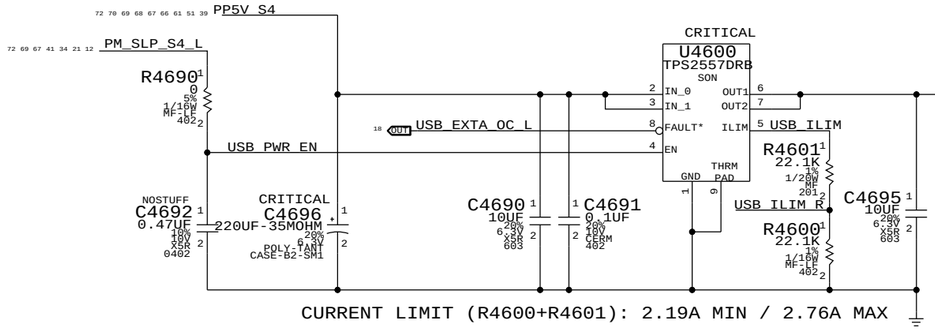
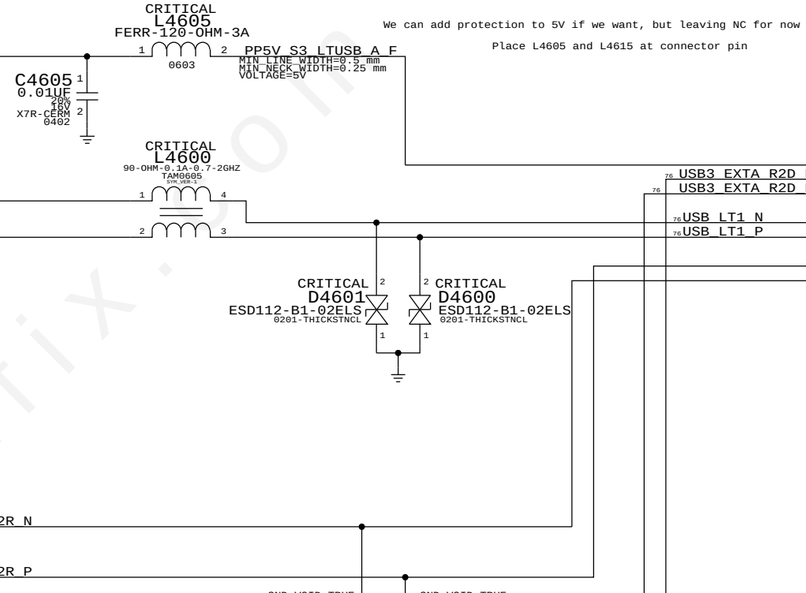
USB Port Power Switch

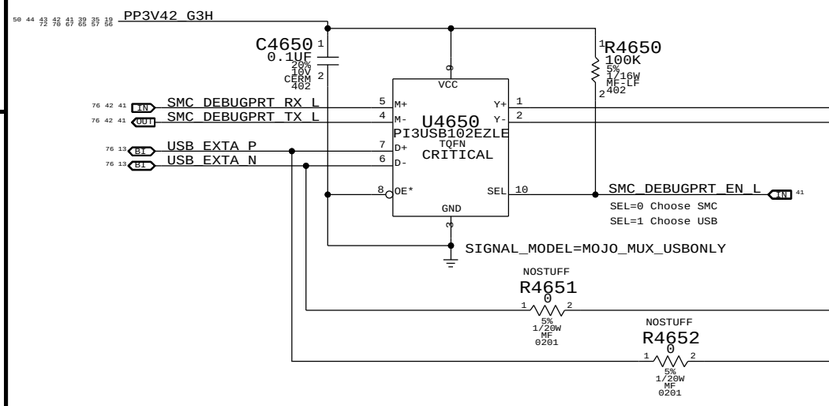


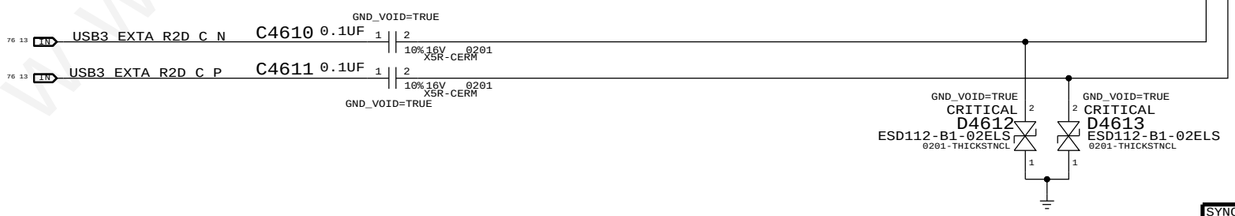
CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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IPD CONNECTOR

CRITICAL
J4801
502250-8041
F-RT-SM

TPAD_SPI_MOSI
TPAD_SPI_MISO
TPAD_SPI_SCLK
TPAD_SPI_INT_L
I2C_IOXP_SDA
I2C_IOXP_SCL
USB_TPAD_N
USB_TPAD_P
PP3V3_S4
SMC_PME_S4_WAKE_L
SMBUS_SMC_2_S3_SCL
TPAD_ACTUATOR_THRMTRIP_L
SMC_ACTUATOR_EN_R_L
TPAD_SPI_CS_L
TPAD_SPI_BUS_EN
TPAD_NC4
IOXP2_INT_L
TPAD_NC3
SMBUS_SMC_2_S3_SDA
TPAD_VBUS_EN
GND_ACTUATOR
PPVIN_S4_TPAD

R4893 100K 5% 1/20W MF 0201 NOSTUFF
R4808 0 5% 1/20W MF 0201
C4801 100PF 5% 25V C0G 0201
C4808 1.0UF 10% 35V CERM-X5R 0402
C4806 0.1UF 10% 35V CER-X5R 0201
C4807 0.1UF 10% 35V CER-X5R 0201
R4890 0 5% 1/10W MF-LF 402 NOSTUFF
R4891 0 5% 1/10W MF-LF 402 NOSTUFF
R4809 0 5% 1/20W MF 0201
C4809 100PF 5% 25V C0G 0201 NOSTUFF
XW4801 SM
L4803 FERR-120-OHM-1.5A 0402-LF
C4803 0.1UF 20% 10V CERM 402
R4814 113 1% 1/10W MF-LF 402
R4815 0 5% 1/10W MF-LF 402
R4810 1K 5% 1/10W MF-LF 402
C4810 0.1UF 20% 10V CERM 402

PLACE_NEAR=J4801.35:5mm
PLACE_NEAR=J4801.26:2MM
PLACE_NEAR=J4801:3MM
PLACE_NEAR=J4813.5:5MM
PLACE_NEAR=C4809.1:2MM

PP5V_S4_TPAD_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V

Keyboard Connector

518S0752
CRITICAL
J4813

WS_KBD1 … WS_KBD23
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
WS_KBD15_C
WS_KBD16N

F-RT-SM
FF14A-30C-R11DL-B-3H

SMC Manual Reset & Isolation

LEFT SHIFT, OPTION & CONTROL KEYS COMBINED WITH POWER BUTTON CAUSE SMC RESET# ASSERTION.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

PP3V42_G3H
BYPASS=U4850.10:5:5 mm
C4850 0.1UF 10% 16V X7R-CERM 0402
U4850
SLG4AP4103
TQFN
VDD
GND
THRM PAD

PP3V3_S4
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KEY
SMC_TPAD_RST_L
Pull-up in U5110.

IO EXPANDER / KEYBOARD INTERFACE

U4820
PCAL6416A
VFBGA

R4821 10K 5% 1/20W MF 0201
R4820 100K 5% 1/20W MF 0201
R4822 2.0K 5% 1/20W MF 0201
R4823 2.0K 5% 1/20W MF 0201
C4820 1UF 10% 6.3V CERM 402
C4821 0.1UF 10% 6.3V CERM-X5R 0201
C4822 0.1UF 10% 6.3V CERM-X5R 0201
C4824 0.01UF 10% 16V X5R-CERM 0201 NOSTUFF
R4824 0 5% 1/20W MF 0201 NOSTUFF
Q4840 DMN32D2LFB4 DFN1006H4-3
R4840 100K 1% 1/16W MF-LF 402

IOXP1_INT_L
I2C_IOXP_SCL
I2C_IOXP_SDA
IOXP1_RESET_L
TP_IOXP1_0 … TP_IOXP1_4
IOXP1_DEBUG
WS_KBD16N
IOXP1_LED_DRV
SMC_ONOFF_L

311S0597
(Write: 0x40 Read: 0x41)

U4830
PCAL6416A
VFBGA

R4831 10K 5% 1/20W MF 201
R4830 100K 5% 1/20W MF 201
C4830 1UF 10% 6.3V CERM 402
C4831 0.1UF 10% 6.3V CERM-X5R 0201
C4832 0.1UF 10% 6.3V CERM-X5R 0201
C4834 0.01UF 10% 16V X5R-CERM 0201 NOSTUFF

IOXP2_INT_L
I2C_IOXP_SCL
I2C_IOXP_SDA
IOXP2_RESET_L

R4802 … R4857 10K 5% 1/20W MF 201

311S0597
(Write: 0x42 Read: 0x43)

R4858 … R4862 10K 5% 1/20W MF 201

BYPASS=U4830.B4:E2:5MM
BYPASS=U4830.B3:E2:2MM
BYPASS=U4830.B4:E2:2MM
BYPASS=U4820.B4:E2:5MM
BYPASS=U4820.B4:E2:2MM

SYNC_MASTER=CLEAN_X305_PEG
SYNC_DATE=02/18/2014

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

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DRAWING NUMBER	<SCH_NUM>
SIZE	D
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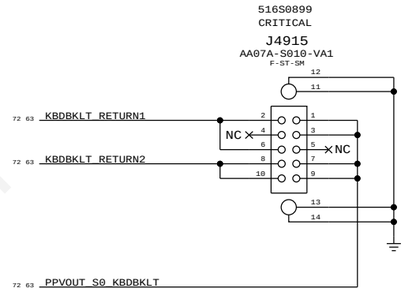
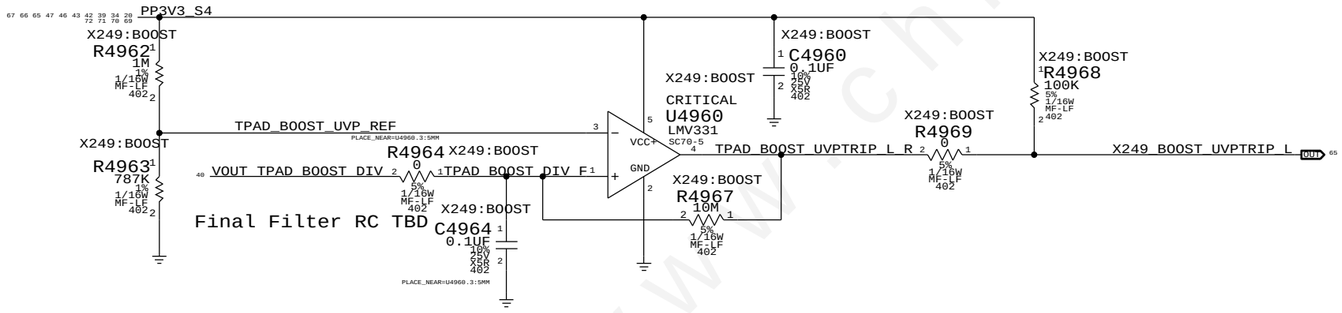
Keyboard Backlight Connector

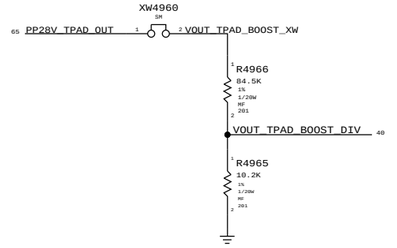


X249 BOOST UVP TRIP



Trip set at 13.5V (divider set for 1.45V)

X249 Boost Voltage Sense



SYNC_MASTER=CLEAN_X305	SYNC_DATE=05/30/2014
PAGE TITLE	KEYBOARD/TRACKPAD (2 OF 2)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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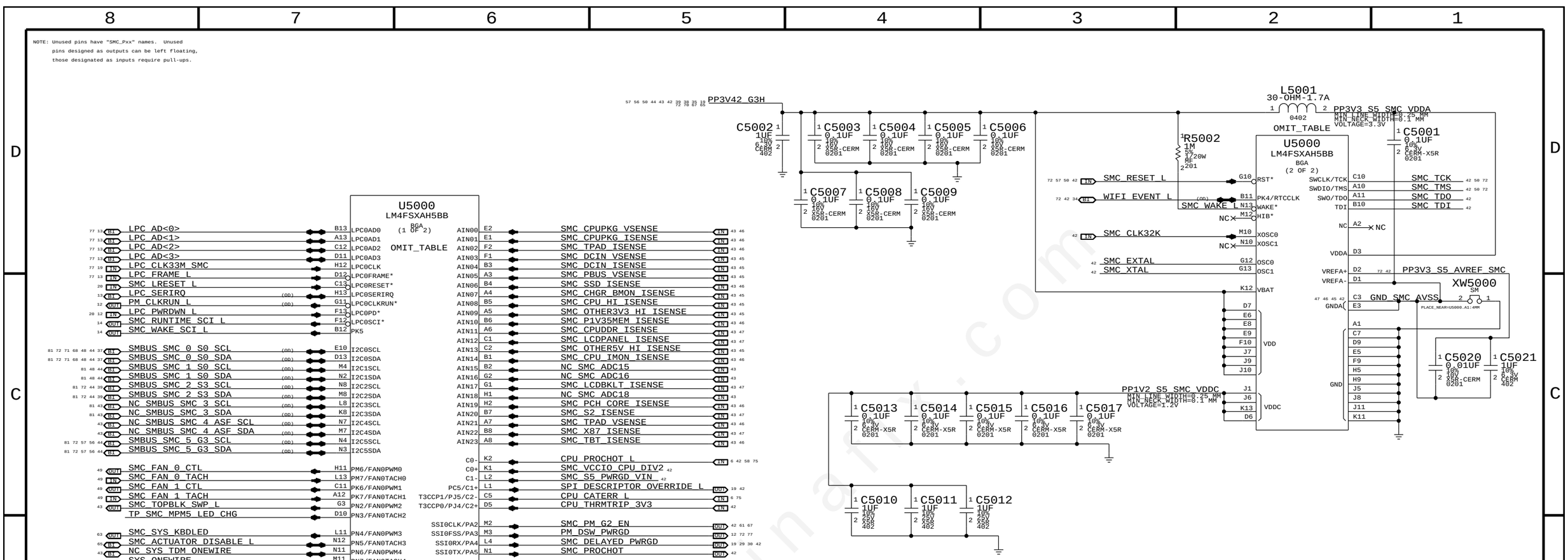
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CLEAN_X305	SYNC_DATE=01/15/2014
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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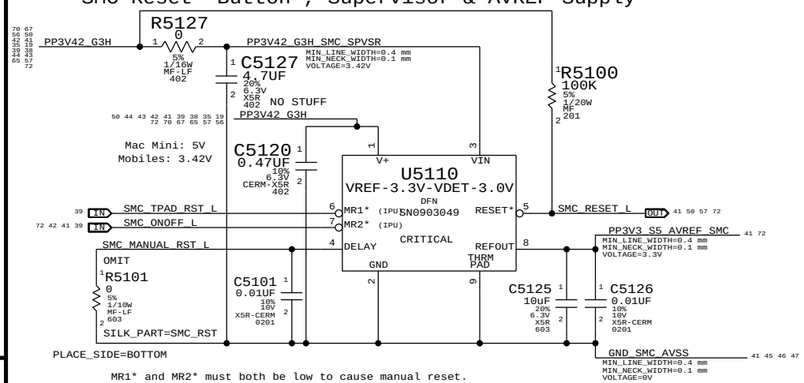
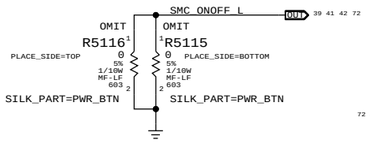
SMC Reset "Button", Supervisor & AVREF Supply



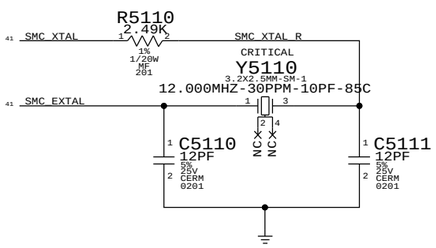
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

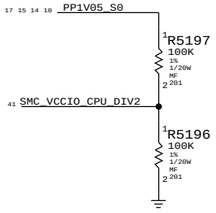
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



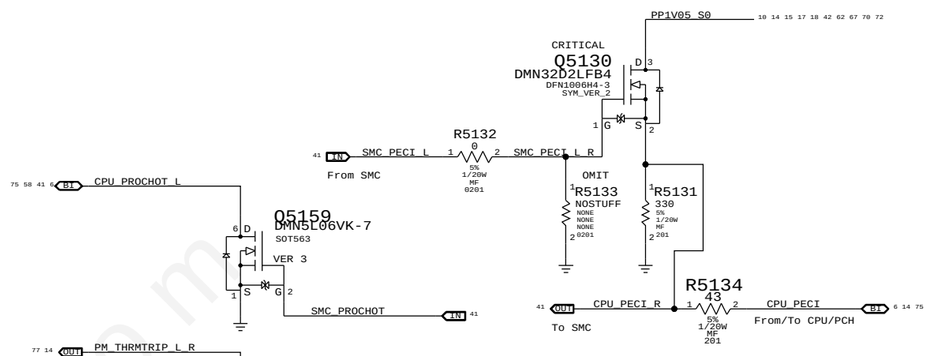
SMC Crystal Circuit

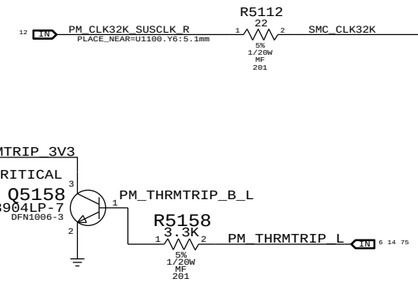




SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

SMC12 PECI SUPPORT





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PAGE TITLE
SMC Shared Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 51 OF 118
SHEET 42 OF 82

8	7	6	5	4	3	2	1

D

C

B

A

SMC_BC_ACOK — SMC_BC_ACOK (MAKE_BASE=TRUE)
NC_HISIDE_ISENSE_OC — NC_HISIDE_ISENSE_OC (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_CPUPKG_VSENSE — SMC_CPUPKG_VSENSE (MAKE_BASE=TRUE)
SMC_CPUPKG_ISENSE — SMC_CPUPKG_ISENSE (MAKE_BASE=TRUE)
SMC_TPAD_ISENSE — SMC_TPAD_ISENSE (MAKE_BASE=TRUE)
SMC_DCIN_VSENSE — SMC_DCIN_VSENSE (MAKE_BASE=TRUE)
SMC_DCIN_ISENSE — SMC_DCIN_ISENSE (MAKE_BASE=TRUE)
SMC_PBUS_VSENSE — SMC_PBUS_VSENSE (MAKE_BASE=TRUE)
SMC_SSD_ISENSE — SMC_SSD_ISENSE (MAKE_BASE=TRUE)
SMC_CHGR_BMON_ISENSE — SMC_CHGR_BMON_ISENSE (MAKE_BASE=TRUE)
SMC_CPU_HI_ISENSE — SMC_CPU_HI_ISENSE (MAKE_BASE=TRUE)
SMC_OTHER3V3_HI_ISENSE — SMC_OTHER3V3_HI_ISENSE (MAKE_BASE=TRUE)
SMC_P1V35MEM_ISENSE — SMC_P1V35MEM_ISENSE (MAKE_BASE=TRUE)
SMC_CPUDDR_ISENSE — SMC_CPUDDR_ISENSE (MAKE_BASE=TRUE)
SMC_LCDPANEL_ISENSE — SMC_LCDPANEL_ISENSE (MAKE_BASE=TRUE)
SMC_OTHER5V_HI_ISENSE — SMC_OTHER5V_HI_ISENSE (MAKE_BASE=TRUE)
SMC_CPU_IMON_ISENSE — SMC_CPU_IMON_ISENSE (MAKE_BASE=TRUE)
NC_SMC_ADC15 — NC_SMC_ADC15 (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ADC16 — NC_SMC_ADC16 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_LCDBKLT_ISENSE — SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE)
NC_SMC_ADC18 — NC_SMC_ADC18 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_PCH_CORE_ISENSE — SMC_PCH_CORE_ISENSE (MAKE_BASE=TRUE)
SMC_S2_ISENSE — SMC_S2_ISENSE (MAKE_BASE=TRUE)
SMC_TPAD_VSENSE — SMC_TPAD_VSENSE (MAKE_BASE=TRUE)
SMC_X87_ISENSE — SMC_X87_ISENSE (MAKE_BASE=TRUE)
SMC_TBT_ISENSE — SMC_TBT_ISENSE (MAKE_BASE=TRUE)
NC_SMBUS_SMC_4_ASF_SCL — NC_SMBUS_SMC_4_ASF_SCL (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_4_ASF_SDA — NC_SMBUS_SMC_4_ASF_SDA (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_3_SCL — NC_SMBUS_SMC_3_SCL (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_3_SDA — NC_SMBUS_SMC_3_SDA (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_TPAD_BOOST_DISABLE — SMC_TPAD_BOOST_DISABLE_L (MAKE_BASE=TRUE)
SMC_PME_S4_DARK_L (MAKE_BASE=TRUE) — SMC_PME_S4_DARK_L
SMC_PME_S4_DARK_L

NC_SMC_SYS_LED — NC_SMC_SYS_LED (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_MEM_EVENT_L — NC_MEM_EVENT_L (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_IR_RX_OUT_RC — NC_IR_RX_OUT_RC (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_TDM_ONEWIRE — NC_SYS_TDM_ONEWIRE (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_GFX_THROTTLE_L — NC_SYS_GFX_THROTTLE_L (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_GFX_OVERTEMP — NC_SYS_GFX_OVERTEMP (MAKE_BASE=TRUE NO_TEST=TRUE)

SMC_SUSACK:YES
R5230 0 5% 1/20W MF 201
SMC_PCH_SUSWARN_L (IN) — PCH_SUSWARN_L (OUT)
R5231 0 5% 1/20W MF 201
SMC_PCH_SUSACK_L (IN) — PCH_SUSACK_L (OUT)
SMC_SUSACK:YES

Spare S4 IRQ

PP3V3_S4
R5259 100K 5% 1/20W MF 201
SMC_DP_HPD_L (OUT)

Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99
SM
NC, NC, PP3V42_G3H, SMC_LID_R, NC, NC
R5250 0 5% 1/20W MF 0201
SMC_LID
C5250 0.001UF 10% 50V X7R CERM 0402

PP3V3_S4
R5282 100K 5% 1/20W MF 201
SMC_PME_S4_WAKE_L (IN) — SMC_PME_S4_WAKE_L (OUT) (MAKE_BASE=TRUE)
SMC_PME_S4_WAKE_L (IN)

R5283 1K 5% 1/20W MF 201
SMC_TOPBLK_SWP_L (IN) — PCH_STRP_TOPBLK_SWP_L (OUT)

PM_BATLOW_L (IN) — PM_BATLOW_L (OUT) (MAKE_BASE=TRUE)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

PAGE TITLE: SMC Project Support
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
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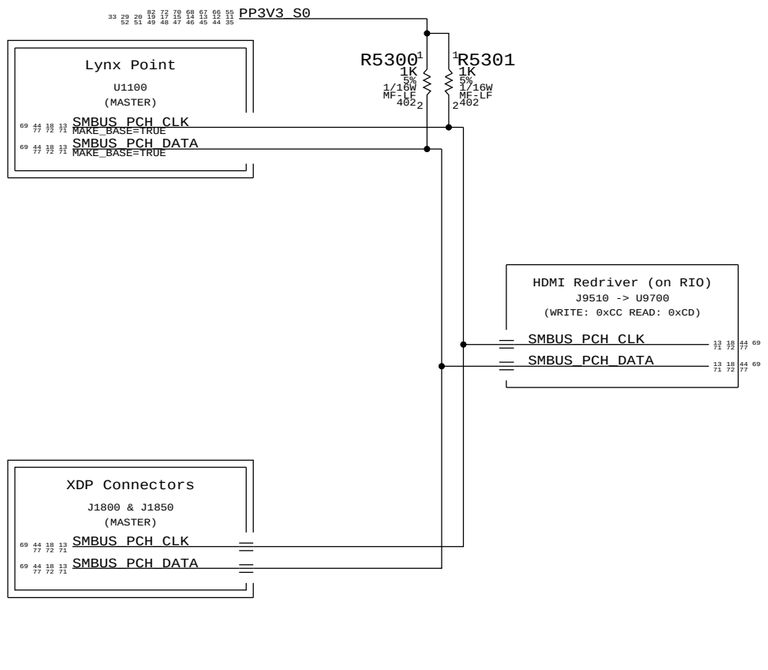
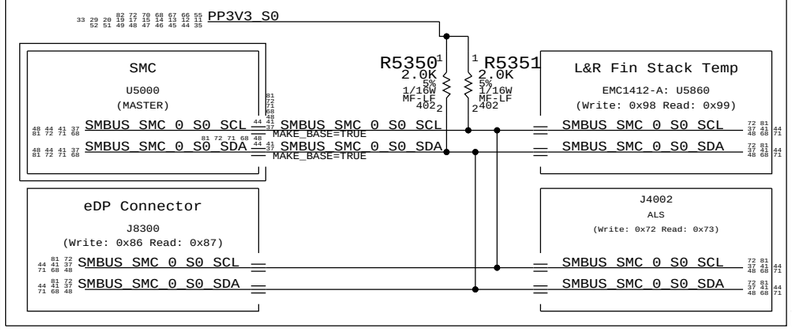
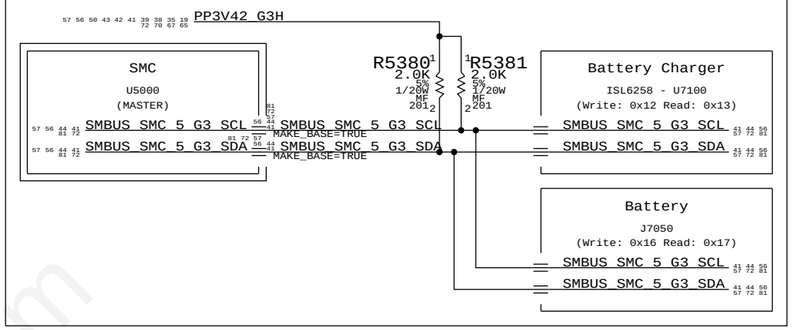
PCH SMBus "0" Connections



SMC "0" SMBus Connections

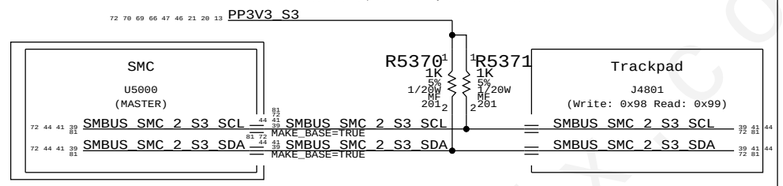


SMC "5" SMBUS CONNECTIONS

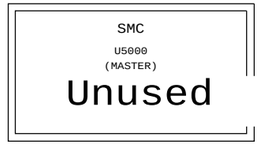


SMC "2" SMBUS CONNECTIONS

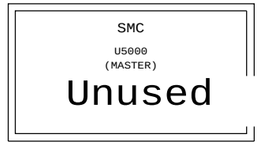
NOTE: SMC RMT bus remains powered and may be active in S3 state



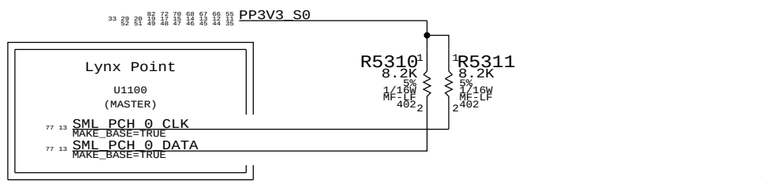
SMC "4" SMBUS CONNECTIONS



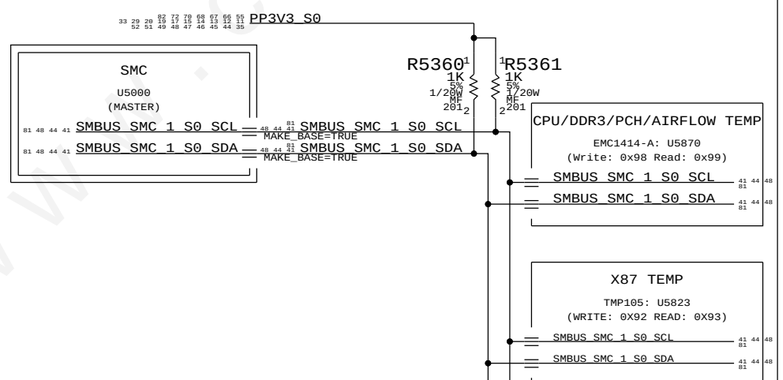
SMC "3" SMBUS CONNECTIONS



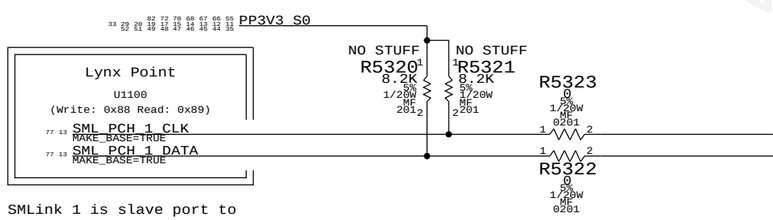
PCH "SMLink 0" Connections



SMC "1" SMBUS CONNECTIONS



PCH "SMLink 1" Connections



SMLink 1 is slave port to
access PCH & CPU via PECI.

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE
SMBus Connections

Apple Inc.

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REVISION <E4LABEL>
BRANCH <BRANCH>
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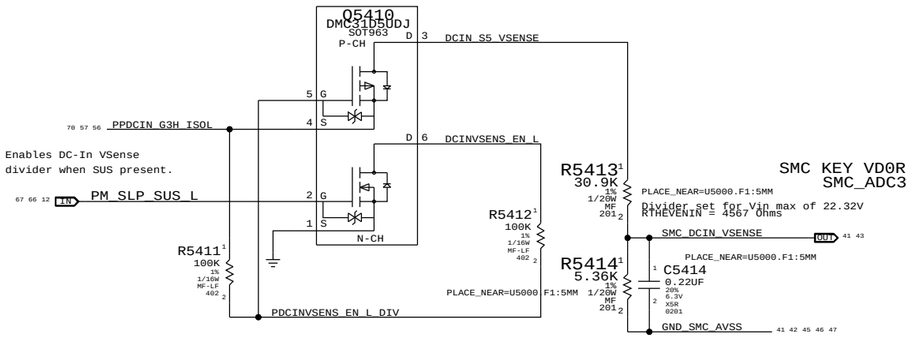
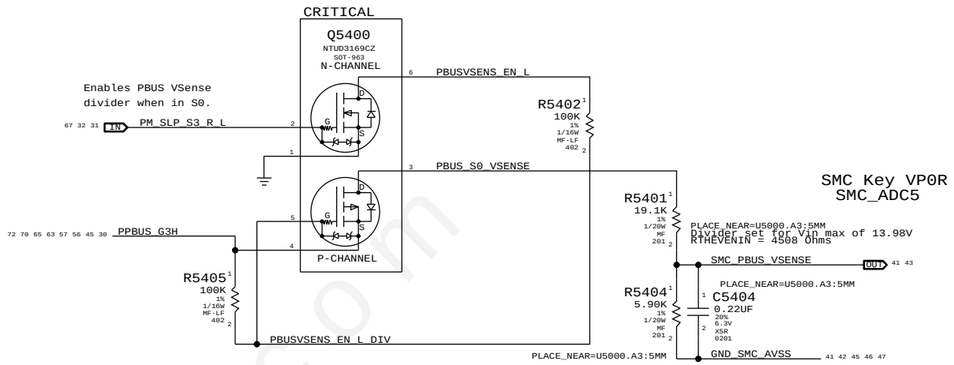
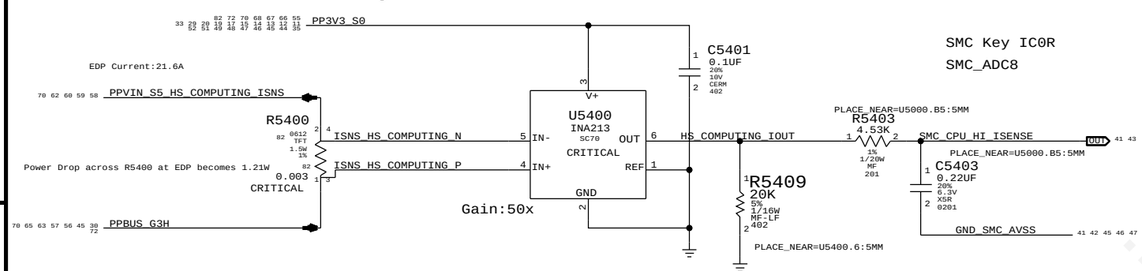
DC-In Voltage Sense Enable & Filter



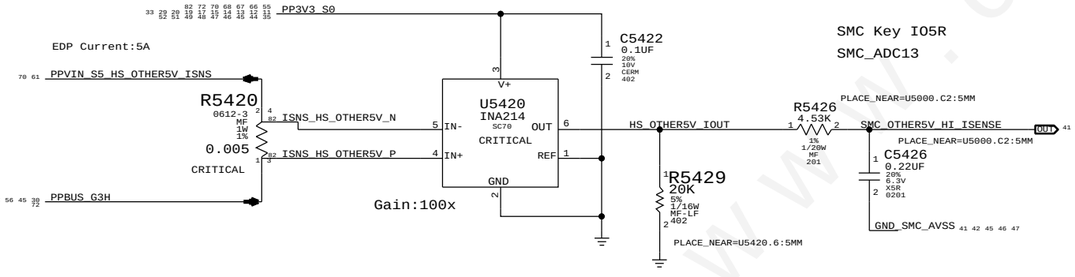
PBUS Voltage Sense Enable & Filter



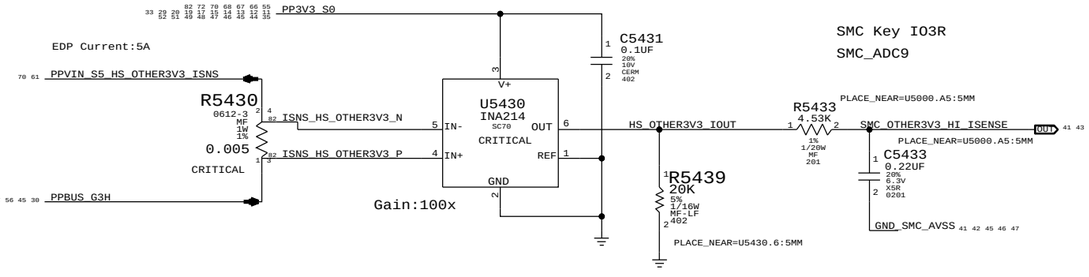
COMPUTING High Side Current Sense / Filter



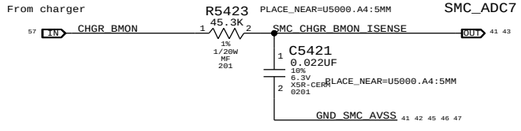
OTHERS (5V) High Side Current Sense / Filter



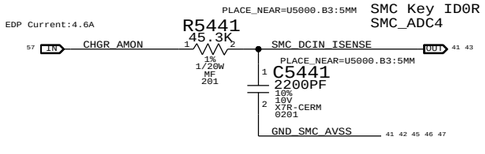
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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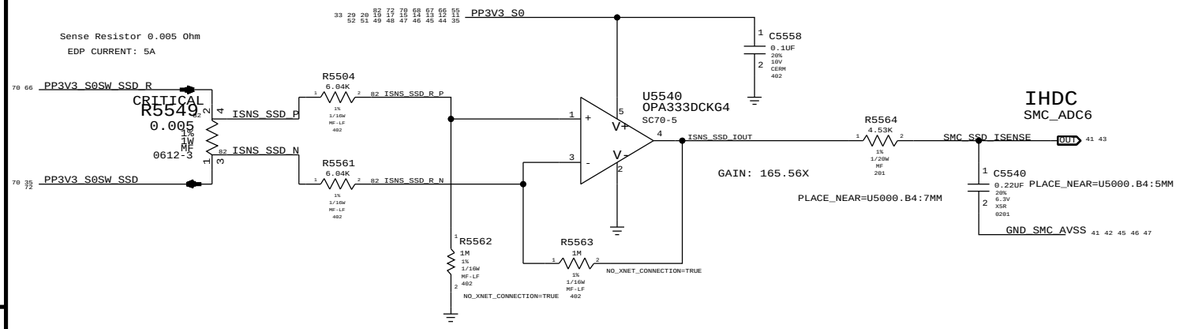
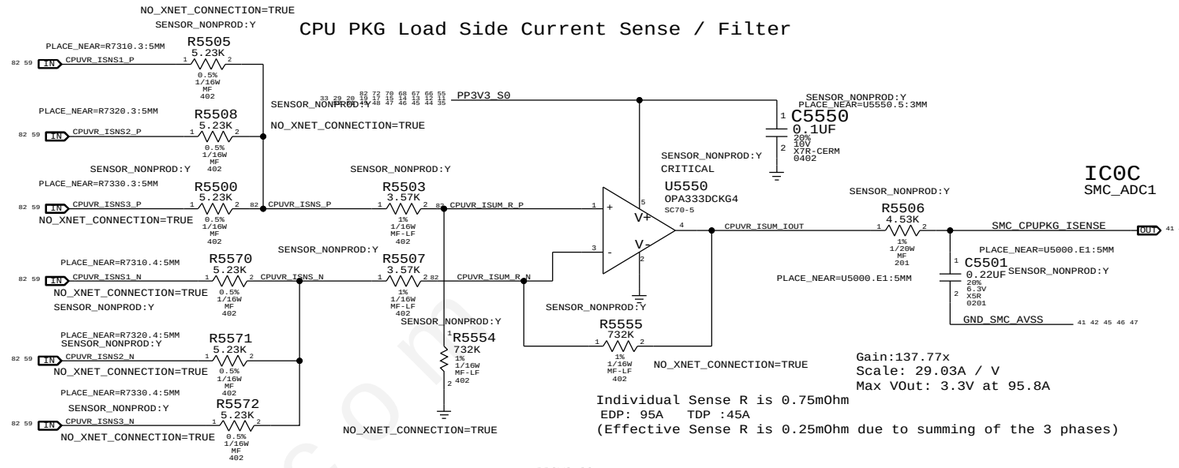
SSD CURRENT SENSE

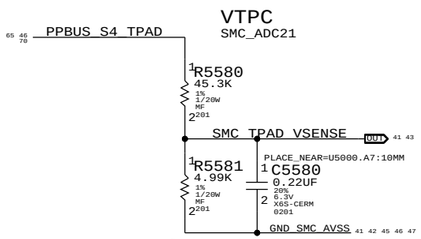


TBT Router CURRENT SENSE

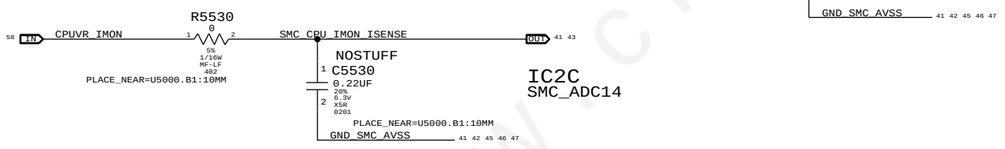
CPU PKG Load Side Current Sense / Filter



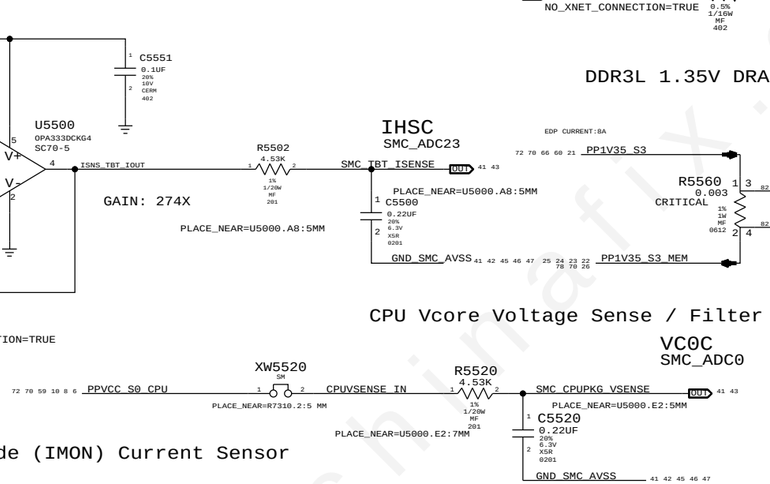
TRACK PAD VOLTAGE SENSE



CPU Load Side (IMON) Current Sensor

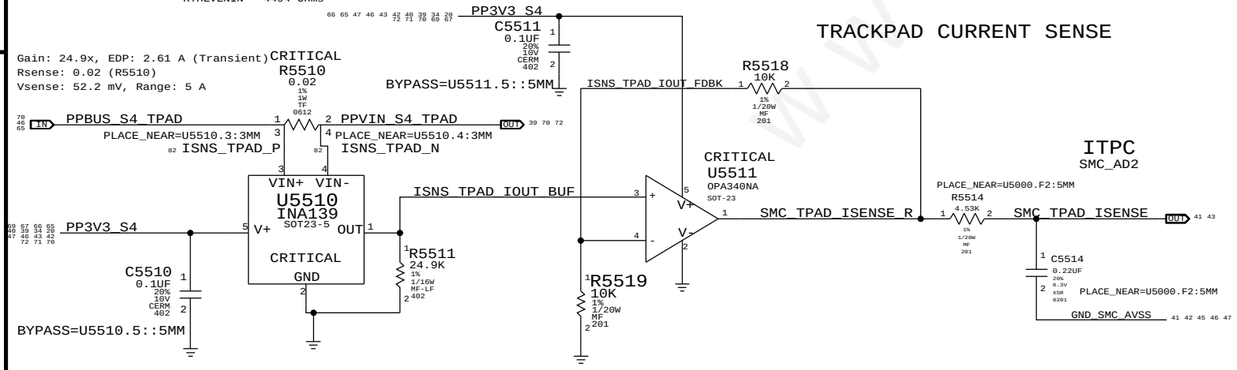


CPU Vcore Voltage Sense / Filter

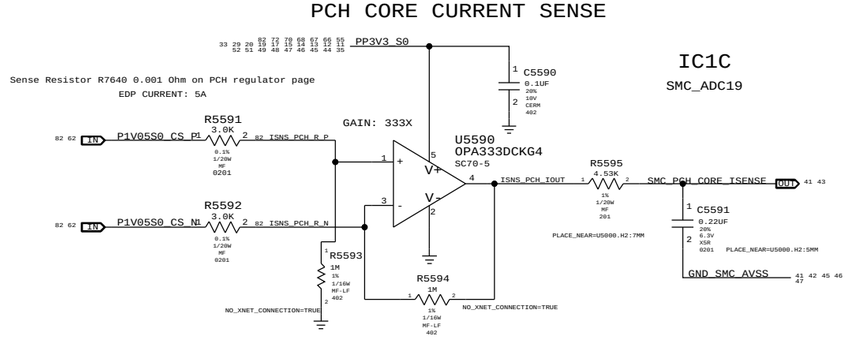


DDR3L 1.35V DRAM ONLY CURRENT SENSE / FILTER

TRACKPAD CURRENT SENSE



PCH CORE CURRENT SENSE



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PAGE TITLE	Load Side Voltage and Current Sensing
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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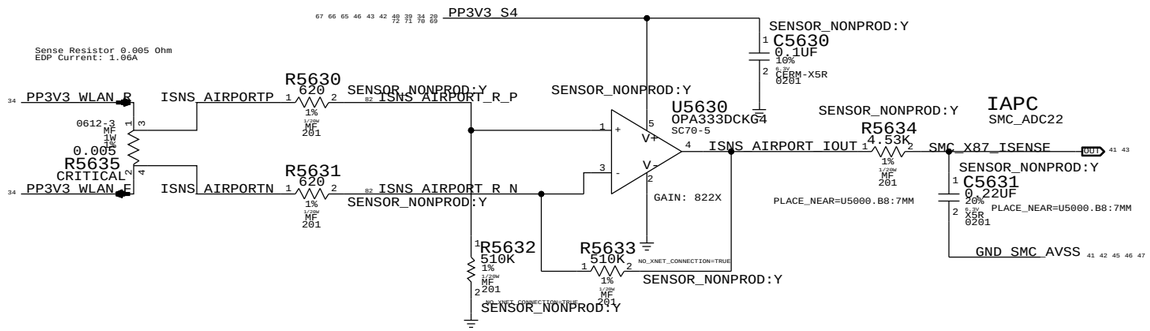
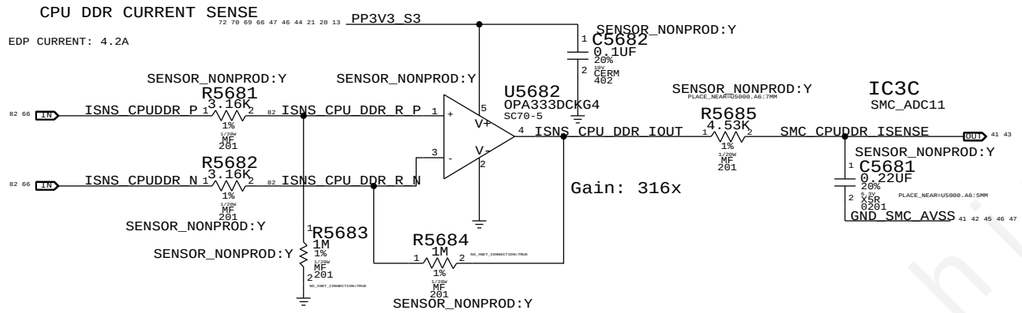
X87 AIRPORT CURRENT SENSE

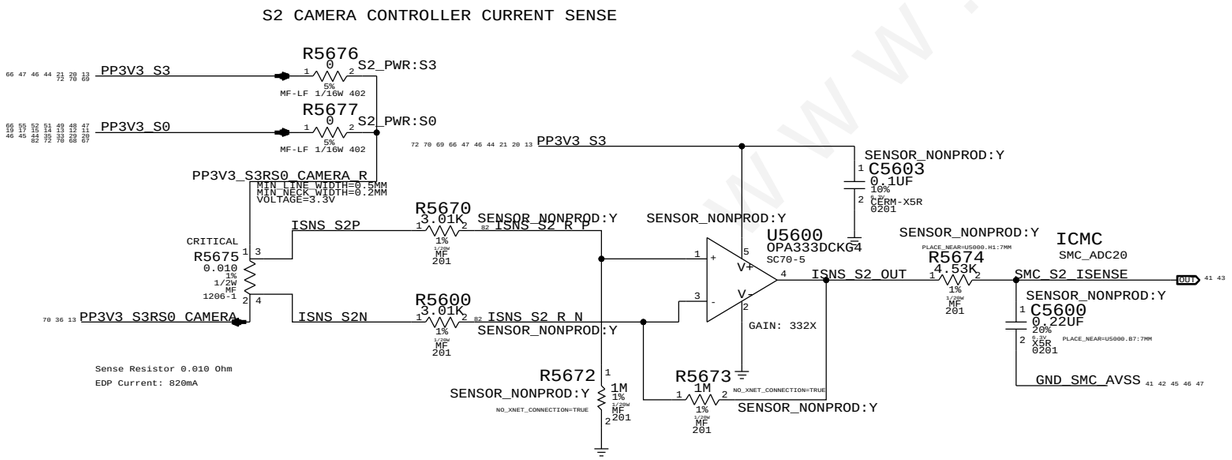


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5601,C5631,C5600,C5681,C5671		SENSOR_NONPROD:N

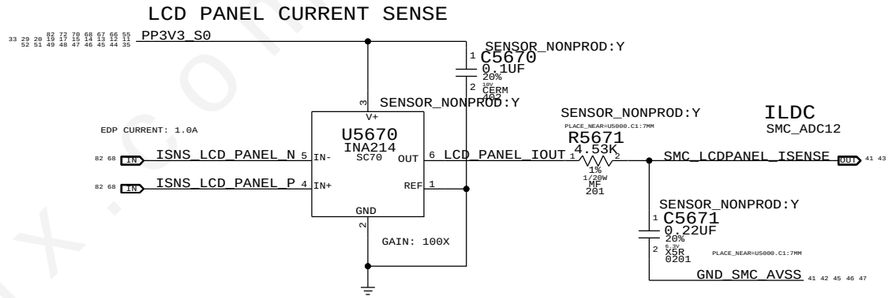
CPU DDR CURRENT SENSE



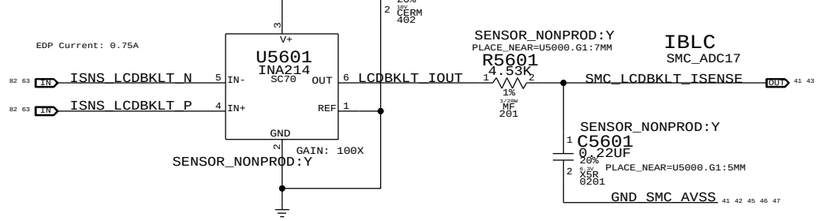
S2 CAMERA CONTROLLER CURRENT SENSE



LCD PANEL CURRENT SENSE



LCD BKLT Current Sense



SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/14/2014

PAGE TITLE: Debug Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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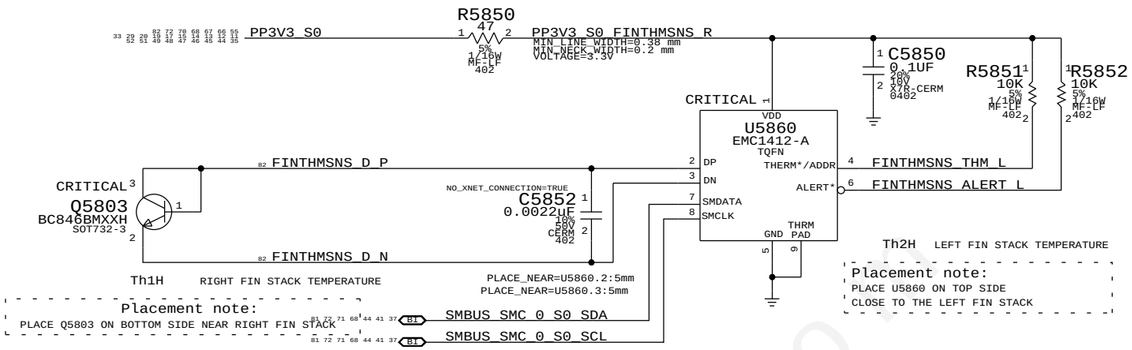
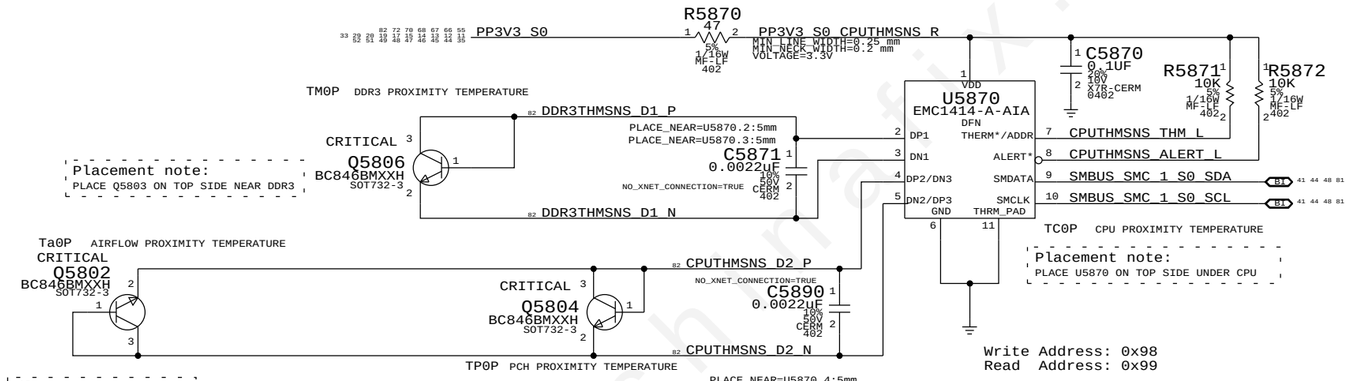
LEFT FIN STACK/RIGHT FIN STACK



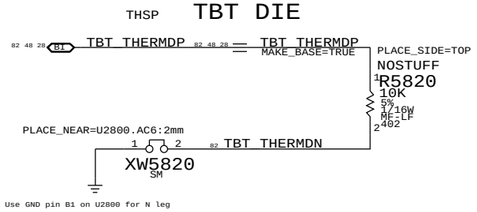
Write Address: 0x98
Read Address: 0x99

DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY

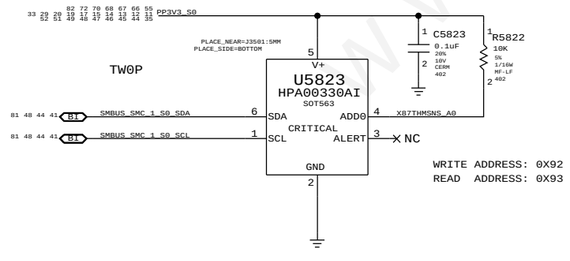


Write Address: 0x98
Read Address: 0x99

TBT DIE



X87 PROXIMITY



SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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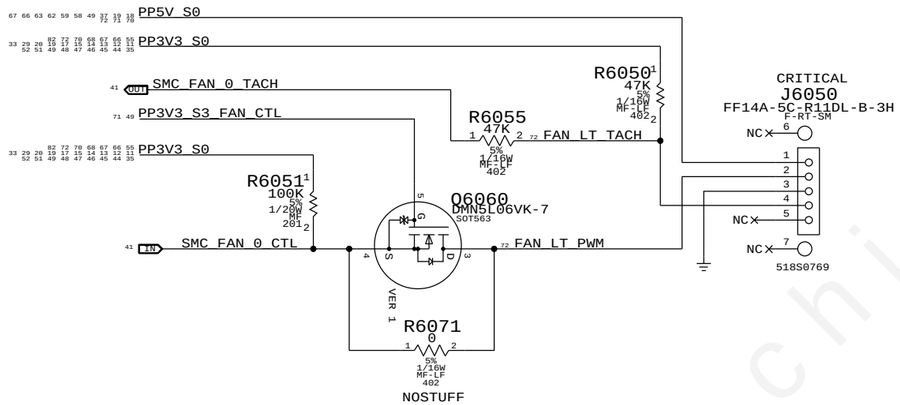
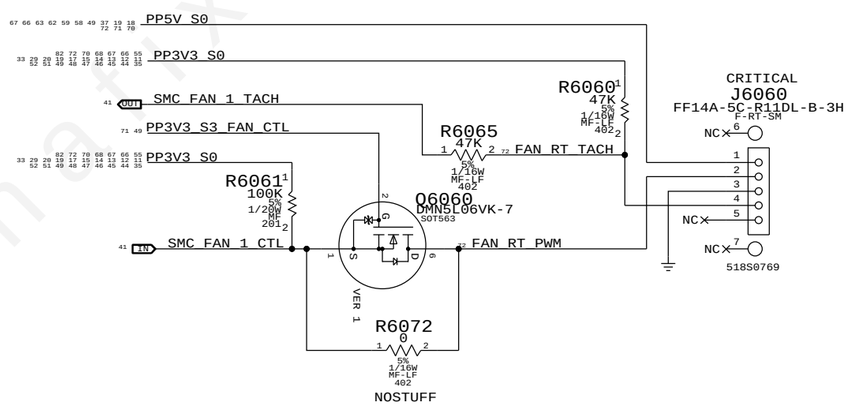
Left Fan



Right Fan



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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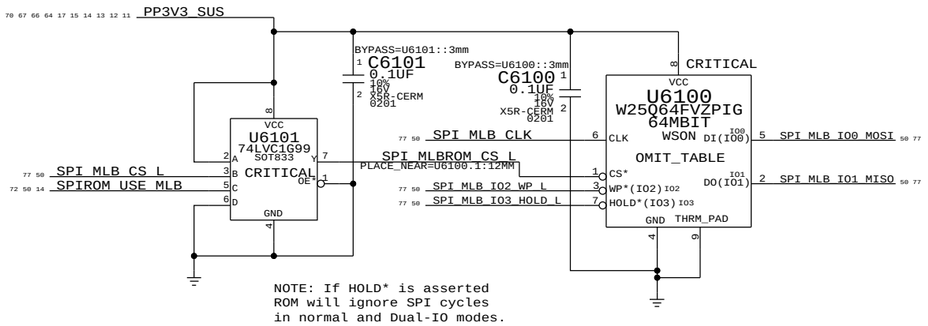
SPI ROM

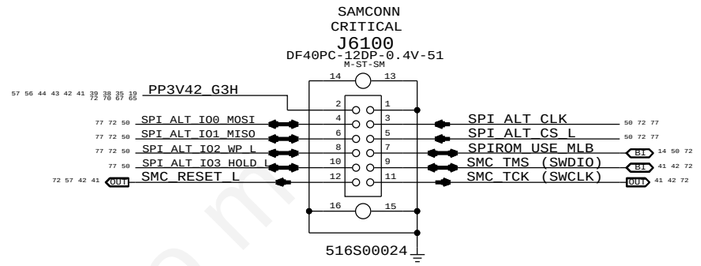
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



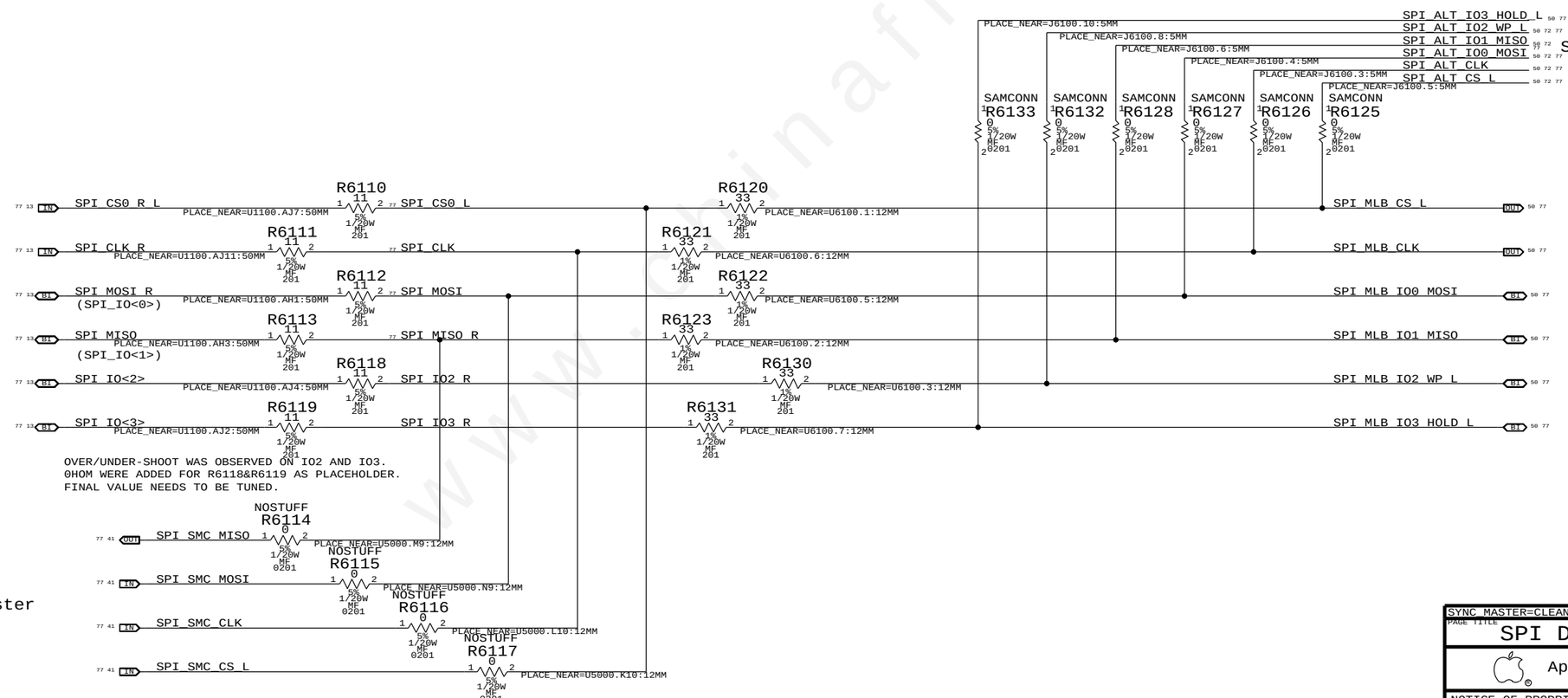
SPI Bus Series Termination

PCH Master

SMC12 Master

Sam Card ROM Slave

SPI ROM Slave



OVER/UNDER-SHOOT WAS OBSERVED ON IO2 AND IO3.
0HOM WERE ADDED FOR R6118&R6119 AS PLACEHOLDER.
FINAL VALUE NEEDS TO BE TUNED.

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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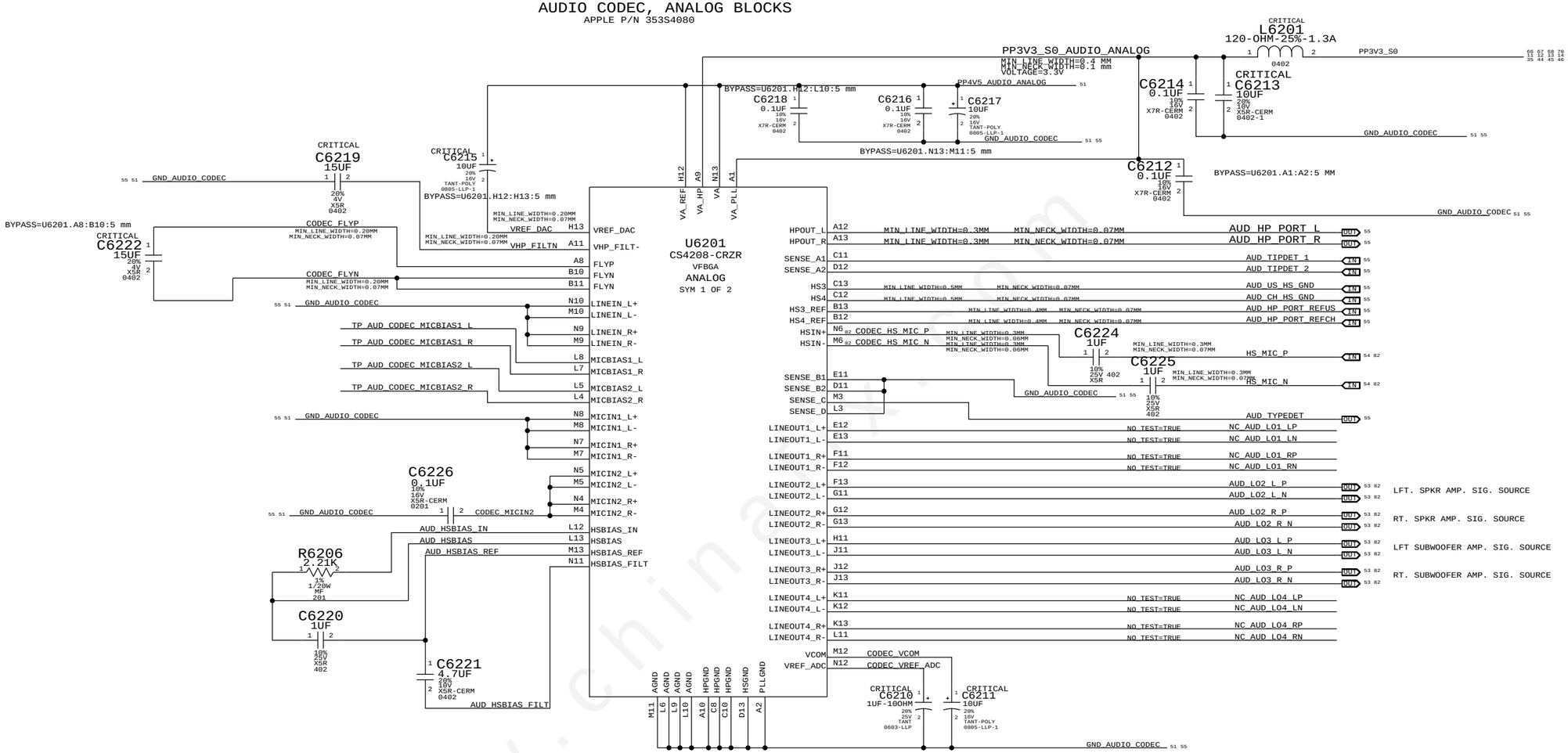
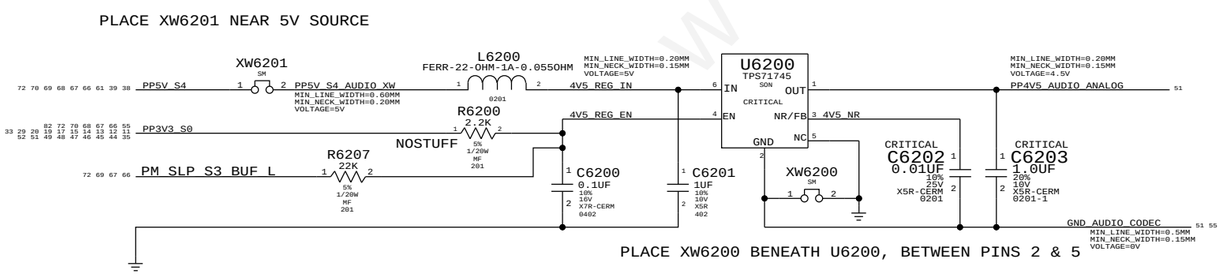
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, ANALOG

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.055OHM
0201

PP1V5_S0 → C6300 4.7UF 20% 4V X5R-1 402 ; C6301 0.1UF 10% 10V X7R-CERM 0201
PP1V5_S0_AUDIO_DIG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.07MM
VOLTAGE=1.5V
BYPASS=U6201.J2:J1:5 mm

C6302 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.E1:F1:5 mm

BYPASS=U6201.G1:F1:5 mm
C6303 0.1UF 10% 6.3V CERM-X5R 0201
C6304 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U6201.K1:K3:5 mm
C6305 10UF 20% 10V X5R-CERM 0402-1

PP3V3_S0
C6306 10UF 20% 10V X5R-CERM 0402-1
C6307 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U6201.A7:E3:5 mm

PP3V3_S0 → R6324 100K 5% 1/20W MF 201 ; R6325 100K 5% 1/20W MF 201

R6323 100K 5% 1/20W MF 201 — PD_CS4208_GPIO1
NOSTUFF R6322 100K 5% 1/20W MF 201

OMIT
R6302 SHORT 402

R6330 33 5% 1/10W MF-LF 402 — SPDIF_OUT_JACK

R6331 22 5% 1/20W MF 201 — TP_CS4208_HDA_SDOUT1

R6332 75 1% 1/10W MF-LF 402 — DMIC_CLK3

U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

VD	J2	
VL_HD	E1	
VL_SP	A7	
VL_IF	G1	
VL_DM	K1	
GPIO0_SPKR_SHUTDOWN	H3	GPIO0
PD_CS4208_GPIO1	H2	GPIO1
SPKRCONN_L_ID	H1	GPIO2
SPKRCONN_R_ID	C4	GPIO3
DFET_OPENUS	C5	GPIO4
DFET_OPENCH	C7	GPIO5
NC_CS4208_GPO0 (NO_TEST=TRUE)	C9	GPO0
NC_CS4208_GPO1 (NO_TEST=TRUE)	B9	GPO1
HDA_BIT_CLK	F2	BCLK
HDA_SYNC	E2	SYNC
HDA_SDIN0	D1	SDI0
CS4208_HDA_SDOUT0_R	C1	SDI1
HDA_SDOUT	D2	SDO0
	C2	SDO1
	C3	SDO2
	B1	SDO3
HDA_RST_L	D3	RST*
NC_CS4208_MCLKA (NO_TEST=TRUE)	A5	MCLK_A
NC_CS4208_SCLKA (NO_TEST=TRUE)	B2	SCLK_A
NC_CS4208_LRCLKA (NO_TEST=TRUE)	B4	LRCK_A
NC_CS4208_SDOUTA (NO_TEST=TRUE)	A3	SDOUT_A
	B3	SDIN_A
NC_CS4208_MCLKB (NO_TEST=TRUE)	A6	MCLK_B
NC_CS4208_SCLKB (NO_TEST=TRUE)	B6	SCLK_B
NC_CS4208_LRCLKB (NO_TEST=TRUE)	B5	LRCK_B
NC_CS4208_SDOUTB (NO_TEST=TRUE)	B8	SDOUT_B
	A4	SDIN_B
	C6	SDA
	B7	SCL
DGND	J1	
LGND	F1	
LGND	E3	
LGND	F3	
LGND	J3	
LGND	K3	
SPDIF_IN	G3	CS4208_SPDIF_IN
SPDIF_OUT	G2	CS4208_SPDIF_OUT
DMIC_SDA0	N3	
DMIC_SCL0	N2	NC_DMIC_CLK0 (NO_TEST=TRUE)
DMIC_SDA1	N1	
DMIC_SCL1	M1	NC_DMIC_CLK1 (NO_TEST=TRUE)
DMIC_SDA2	M2	
DMIC_SCL2	L1	NC_DMIC_CLK2 (NO_TEST=TRUE)
DMIC_SDA3	K2	
DMIC_SCL3	L2	
NC	F6	
NC	F7	
NC	F8	
NC	G6	
NC	G7	
NC	G8	
NC	H6	
NC	H7	
NC	H8	

DMIC_SDA3 → PP6301 P3MMSM
PLACE_NEAR=U6201.N3:5 mm

HDA_BIT_CLK → PP6302 P3MMSM
PLACE_NEAR=U6201.F2:5 mm

HDA_SYNC → PP6303 P3MMSM
PLACE_NEAR=U6201.E2:5 mm

HDA_SDOUT → PP6304 P3MMSM
PLACE_NEAR=U6201.D2:5 mm

CS4208_HDA_SDOUT0_R → PP6305 P3MMSM
PLACE_NEAR=U6201.D1:5 mm

SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

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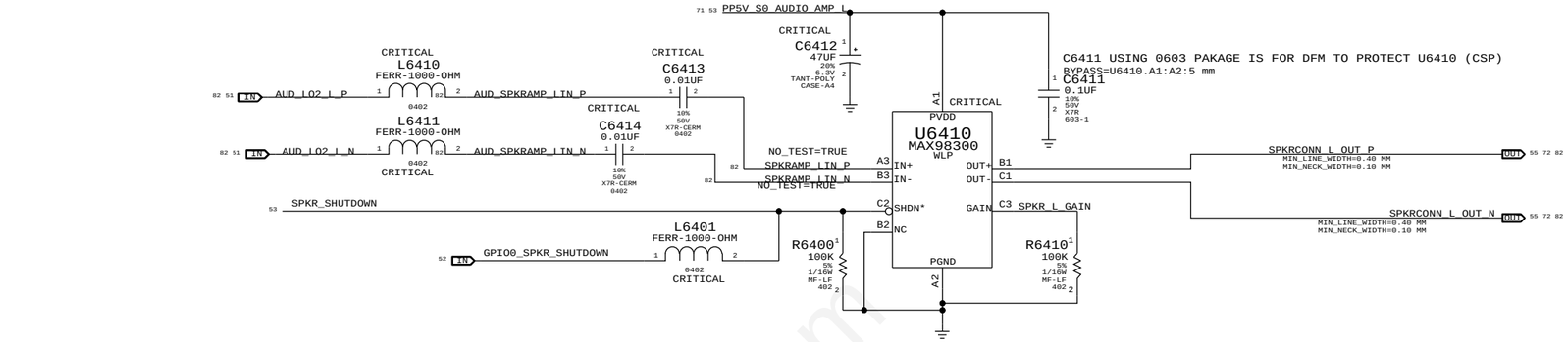
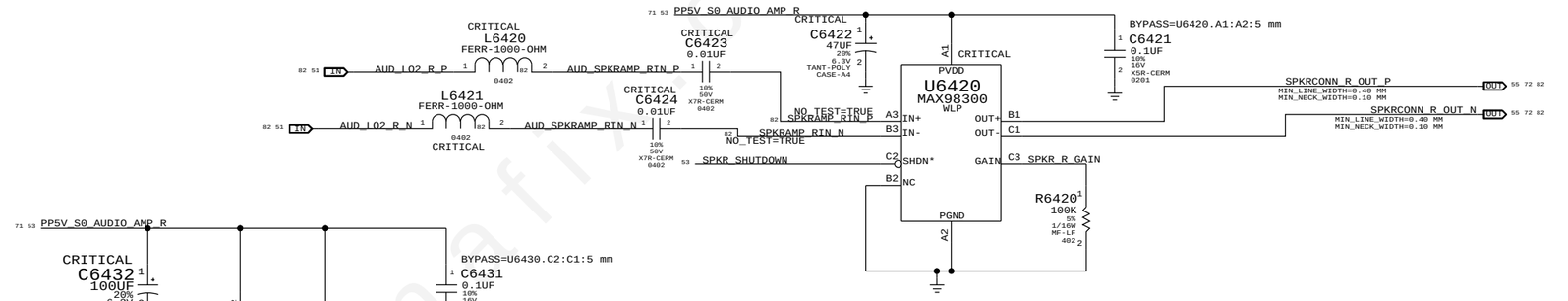
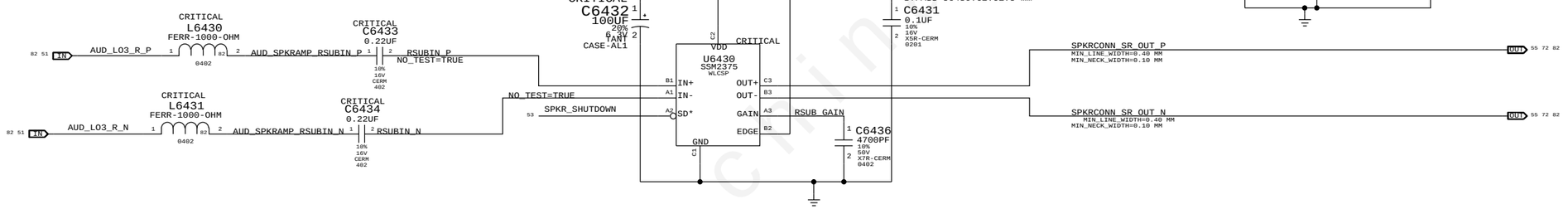
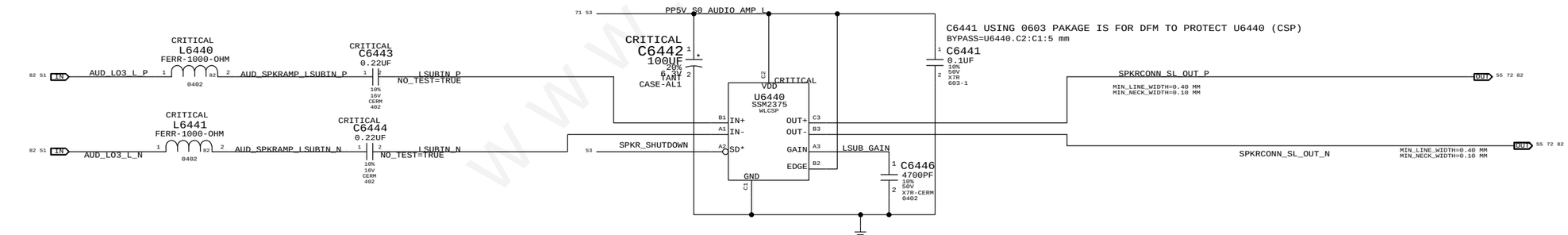
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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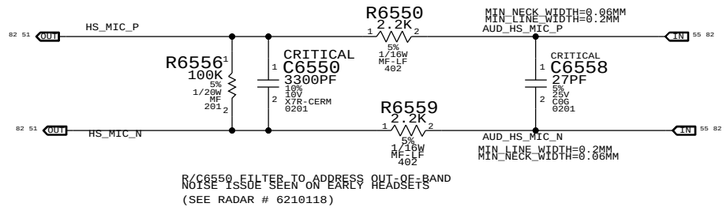
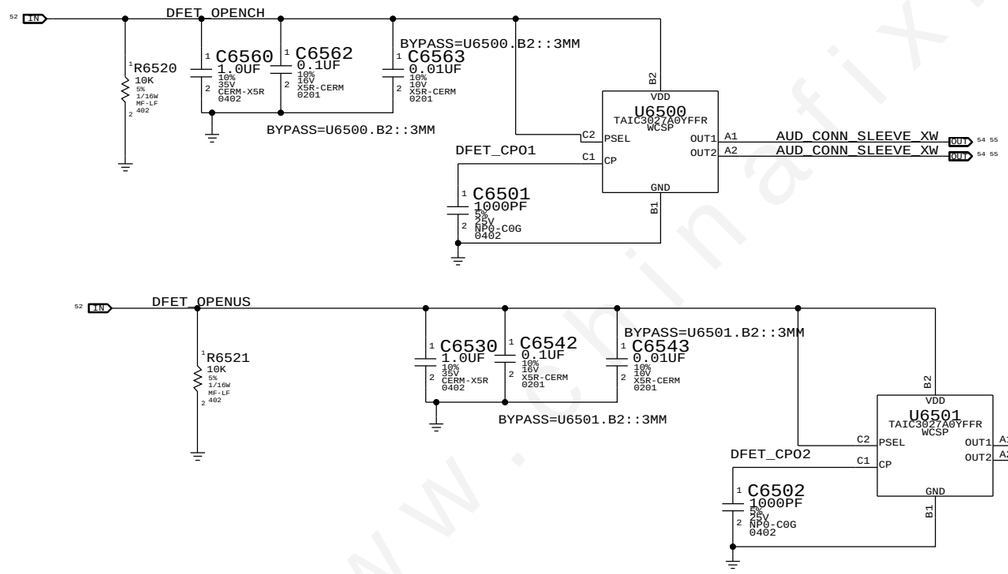


R/C6550 FILTER TO ADDRESS OUT-OF-BAND
NOISE ISSUE SEEN ON EARLY HEADSETS
(SEE RADAR # 6210118)



SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE
AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

PP3V3_S0
DMIC_SDA3
DMIC_CLK3
OMIT
R6680
SHORT
DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

L6611 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM

XW6600 SM PLACE_NEAR=J6600.3:2.54mm

L6612 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CH_HS_GND
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM

XW6601 SM
AUD_HS_MIC_P

L6613 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM

XW6602 SM PLACE_NEAR=J6600.5:2.54mm

L6614 120-OHM-25%-1.3A 0402 CRITICAL
AUD_US_HS_GND
AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM

XW6603 SM
AUD_HS_MIC_N

L6604 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM

R6602 2.2K 5% 1/20W MF 201
GND_AUDIO_CODEC
R6603 2.2K 5% 1/20W MF 201

L6608 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_2
AUD_CONN_TIPDET_2

L6607 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_1
AUD_CONN_TIPDET_1

L6605 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM

L6606 FERR-470-OHM 0201 CRITICAL
AUD_TYPEDET
AUD_CONN_TYPEDET

SPDIF_OUT_JACK
PP3V3_S0

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC
SHELL PINS

VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF

C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

R6601 10K 5% 1/16W MF-LF 402

DZ6607 ESDALC5-1BM2 SOD882 CRITICAL
DZ6601 ESDALC5-1BM2 SOD882 CRITICAL
DZ6602 ESDALC5-1BM2 SOD882 CRITICAL
DZ6603 ESDALC5-1BM2 SOD882 CRITICAL
DZ6606 ESDALC5-1BM2 SOD882 CRITICAL
DZ6605 ESDALC5-1BM2 SOD882 CRITICAL
DZ6604 ESDALC5-1BM2 SOD882 CRITICAL

C6602 100PF 5% 25V C0G 0201
C6603 100PF 5% 25V C0G 0201
C6604 100PF 5% 25V C0G 0201
C6605 100PF 5% 25V C0G 0201
C6606 100PF 5% 25V C0G 0201
C6607 100PF 5% 25V C0G 0201
C6608 100PF 5% 25V C0G 0201

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

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MagSafe DC Power Jack

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM
518S0508

72 PP20V_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=20V

CRITICAL
F7005
6AMP-32V-0.00950HM
0603

PPDCIN_G3H 57 70 72

NOSTUFF
C7005 0.01UF 20% 50V CERM 0603

TP_TDM_ONEWIRE_MPM

PP3V42_G3H 67 70 72 43 44 50 56 57 65

C7008 0.1UF 20% 10V CERM 402
PLACEMENT_NOTE=PLACE NEAR U7100 and U7001

CRITICAL
U7001
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK_VCC

SMC_BC_ACOK IN 41 42 43 57

C7000 0.1UF 20% 10V CERM 402

R7029 2.0K 5% 1/16W MF-LF 402

VCC

U7000
MAX9940
SC70-5
CRITICAL

72 ADAPTER_SENSE

EXT INT

SYS_ONEWIRE BI 41

NC GND

NC

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

R7012 22.1K 1% 1/20W MF 201
Input impedance of 22.1K meets sparkitecture requirements for D2 design only

Q7010
SI5419DU
POWERPAK

R7010 100K 5% 1/20W MF 201

C7012 0.047UF 10% 25V X7R 0402

R7011 10K 5% 1/20W MF 201

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

DCIN_ISOL_GATE_R

DCIN_ISOL_GATE

70 57 45 PPDCIN_G3H_ISOL

D7010
CDZ6.8B
SM
6.8V Zener

R7020 47 1% 1/3W MF 805

PP20V_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V

CRITICAL
D7005
BAT30CWFILM
SOT-323

R7005 10 5% 1/8W MF-LF 805

72 70 65 63 57 45 30 PPBUS_G3H

PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=20V

APN:353S3733
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

NOTE: MIRROR C7092 and C7096

NOSTUFF C7090 4.7UF 10% 35V X5R-CERM 0603
NOSTUFF C7091 4.7UF 10% 35V X5R-CERM 0603
C7092 4.7UF 10% 35V X5R-CERM 0603
C7093 4.7UF 10% 35V X5R-CERM 0603
C7096 4.7UF 10% 35V X5R-CERM 0603
C7097 4.7UF 10% 35V X5R-CERM 0603

NOTE: MIRROR C7093 and C7097

P3V42G3H_BOOST
DIDT=TRUE

C7094 0.22UF 10% 10V CERM 402

CRITICAL
L7095
33UH-20%-0.39A-0.435OHM
DP41BC-SM

U7090
LT3470AED
DFN
CRITICAL
VIN BOOST SW BIAS FB THRM GND PAD NC

R7001 0 5% 1/20W MF 0201

P3V42G3H_SHDN_L

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

OMIT
C7001 NOSTUFF NONE NONE NONE 402

NOSTUFF
R7002 49.9K 1% 1/20W MF 201

C7095 22PF 5% 50V C0G 0201

P3V42G3H_BIAS

P3V42G3H_FB

<Ra>
R7095 348K 1% 1/20W MF 201

<Rb>
R7096 200K 1% 1/20W MF 201

Vout = 1.25V * (1 + Ra / Rb)

PP3V42_G3H 19 25 39 39 41 42 43 44 50 56 57 65 67 70 72

Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

NOTE: R7097 can be replaced by SHORT at PVT

R7097 0 5% 1/16W MF-LF 402

C7099 10UF 20% 10V X5R-CERM 0402-1

C7098 10UF 20% 10V X5R-CERM 0402-1

BATTERY CONNECTOR

518-0376
CRITICAL
J7050
BAT-J5
F-ST-TH
VER 1

12 POS 1
13 POS 2
14 POS 3
15 POS 4
16 SCL 5
17 SDA 6
18 SYS_DETECT 7
19 NEG 8
20 NEG 9
21 NEG 10
22 NEG 11

NC NC

72 57 PPVBAT_G3H_CONN

SMBUS_SMC_5_G3_SCL 41 44 57 72 81
SMBUS_SMC_5_G3_SDA 41 44 57 72 81
72 SYS_DETECT_L

C7050 0.1UF 10% 25V X5R 402

C7060 1UF 10% 16V X5R 402

CRITICAL
D7050
RCLAMP2402B
SC-75

R7050 10K 5% 1/16W MF-LF 402

SYNC_MASTER=CLEAN X305 PEG SYNC_DATE=02/18/2014

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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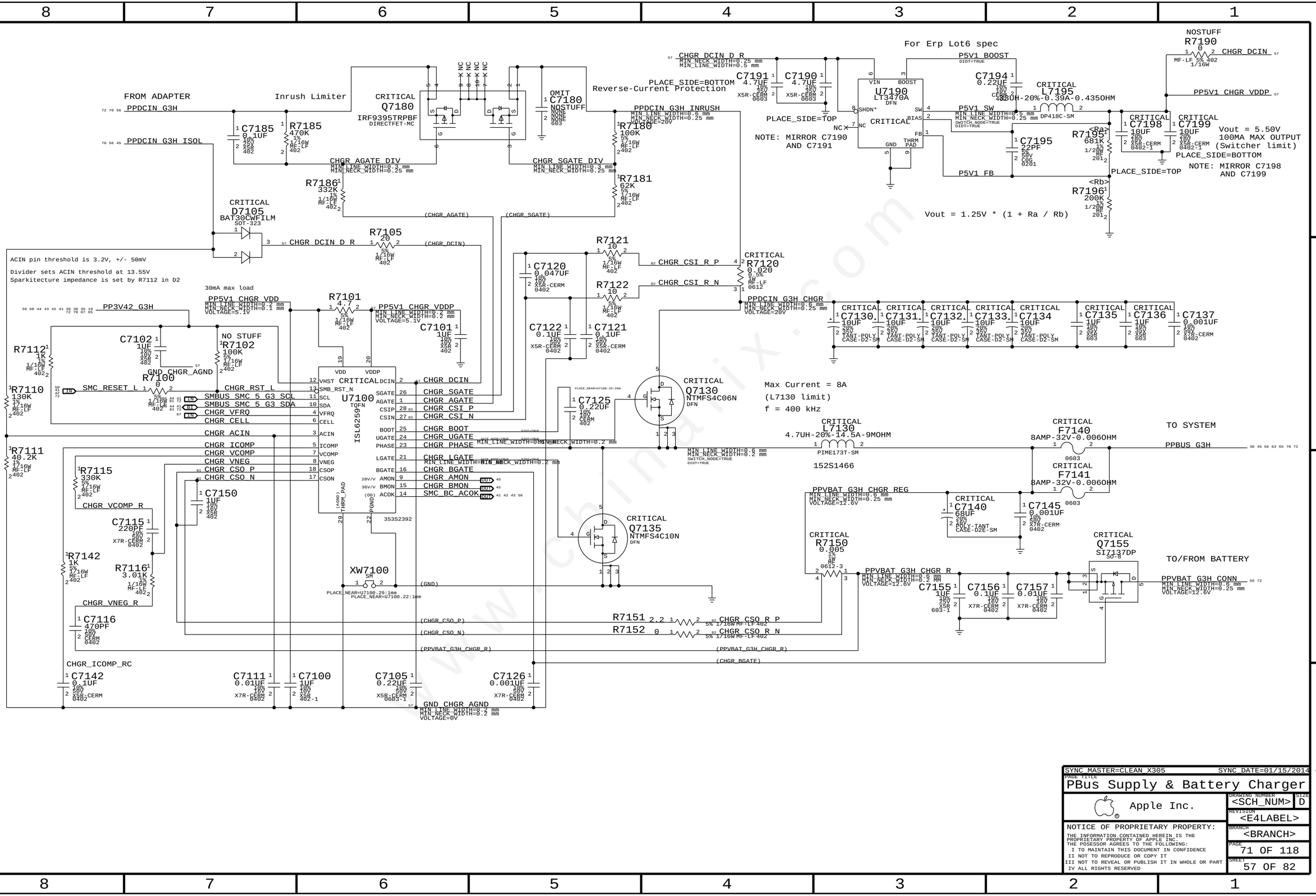
FROM ADAPTER
PPDCIN G3H
PPDCIN G3H ISOL
Inrush Limiter
CRITICAL Q7180 IRF9395TRPBF DIRECTFET-MC
OMIT C7180 NOSTUFF
Reverse-Current Protection
PPDCIN G3H INRUSH
PLACE_SIDE=BOTTOM
CHGR DCIN D R
C7191 4.7UF
C7190 4.7UF
PLACE_SIDE=TOP
NOTE: MIRROR C7190 AND C7191
For Erp Lot6 spec
P5V1 BOOST
U7190 LT3470A DFN
CRITICAL L7195 4.7UH-20%-0.39A-0.435OHM
P5V1 SW
P5V1 FB
C7194 0.22UF
C7195 22PF
R7195 681K
R7196 200K
Vout = 1.25V * (1 + Ra / Rb)
NOSTUFF R7190 0
CHGR DCIN
PP5V1 CHGR VDDP
CRITICAL C7198 10UF
CRITICAL C7199 10UF
Vout = 5.50V
100MA MAX OUTPUT
(Switcher limit)
PLACE_SIDE=BOTTOM
NOTE: MIRROR C7198 AND C7199
PLACE_SIDE=TOP
CHGR AGATE DIV
CHGR SGATE DIV
R7186 332K
R7181 62K
R7180 100K
CRITICAL D7105 BAT30CWFILM SOT-323
R7105 20
(CHGR_AGATE)
(CHGR_SGATE)
(CHGR_DCIN)
ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Sparkitecture impedance is set by R7112 in D2
30mA max load
PP3V42_G3H
PP5V1 CHGR VDD
R7101 4.7
PP5V1 CHGR VDDP
C7101 1UF
R7121 10
R7122 10
CHGR CSI R P
CHGR CSI R N
CRITICAL C7120 0.047UF
CRITICAL R7120 0.020
PPDCIN G3H CHGR
C7122 0.1UF
C7121 0.1UF
CRITICAL C7130 10UF
CRITICAL C7131 10UF
CRITICAL C7132 10UF
CRITICAL C7133 10UF
CRITICAL C7134 10UF
CRITICAL C7135 1UF
CRITICAL C7136 1UF
C7137 0.001UF
R7112 1K
C7102 1UF
NO STUFF R7102 100K
R7100 0
GND CHGR AGND
R7110 130K
SMC RESET L
CHGR RST L
SMBUS SMC 5 G3 SCL
SMBUS SMC 5 G3 SDA
CHGR VFRQ
CHGR CELL
CHGR ACIN
CHGR ICOMP
CHGR VCOMP
CHGR VNEG
CHGR CSO P
CHGR CSO N
R7111 40.2K
R7115 330K
C7150 1UF
CRITICAL U7100 ISL6259 TQFN
VDD
VDDP
VHST
SMB_RST_N
SCL
SDA
VFRQ
CELL
ACIN
ICOMP
VCOMP
VNEG
CSOP
CSON
(AGND) THRM_PAD
PGND
DCIN
SGATE
AGATE
CSIP
CSIN
BOOT
UGATE
PHASE
LGATE
BGATE
AMON
BMON
ACOK
CHGR DCIN
CHGR SGATE
CHGR AGATE
CHGR CSI P
CHGR CSI N
CHGR BOOT
CHGR UGATE
CHGR PHASE
CHGR LGATE
CHGR BGATE
CHGR AMON
CHGR BMON
SMC BC ACOK
C7125 0.22UF
CRITICAL Q7130 NTMFS4C06N DFN
Max Current = 8A
(L7130 limit)
f = 400 kHz
CRITICAL L7130 4.7UH-20%-14.5A-9MOHM
PIME173T-SM
152S1466
CRITICAL F7140 8AMP-32V-0.006OHM
CRITICAL F7141 8AMP-32V-0.006OHM
TO SYSTEM
PPBUS G3H
PPVBAT G3H CHGR REG
CRITICAL C7140 68UF
C7145 0.001UF
CRITICAL R7150 0.005
CRITICAL Q7155 SI7137DP SO-8
TO/FROM BATTERY
PPVBAT G3H CHGR R
C7155 1UF
C7156 0.1UF
C7157 0.01UF
PPVBAT G3H CONN
R7151 2.2
R7152 0
CHGR CSO R P
CHGR CSO R N
C7115 220PF
R7142 1K
R7116 3.01K
CHGR VCOMP R
CHGR VNEG R
C7116 470PF
CHGR ICOMP RC
C7142 0.1UF
C7111 0.01UF
C7100 1UF
C7105 0.22UF
C7126 0.001UF
XW7100 SM
353S2392
GND CHGR AGND
(GND)
(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)
SYNC_MASTER=CLEAN_X305
SYNC_DATE=01/15/2014
PAGE TITLE
PBus Supply & Battery Charger
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 71 OF 118
SHEET 57 OF 82
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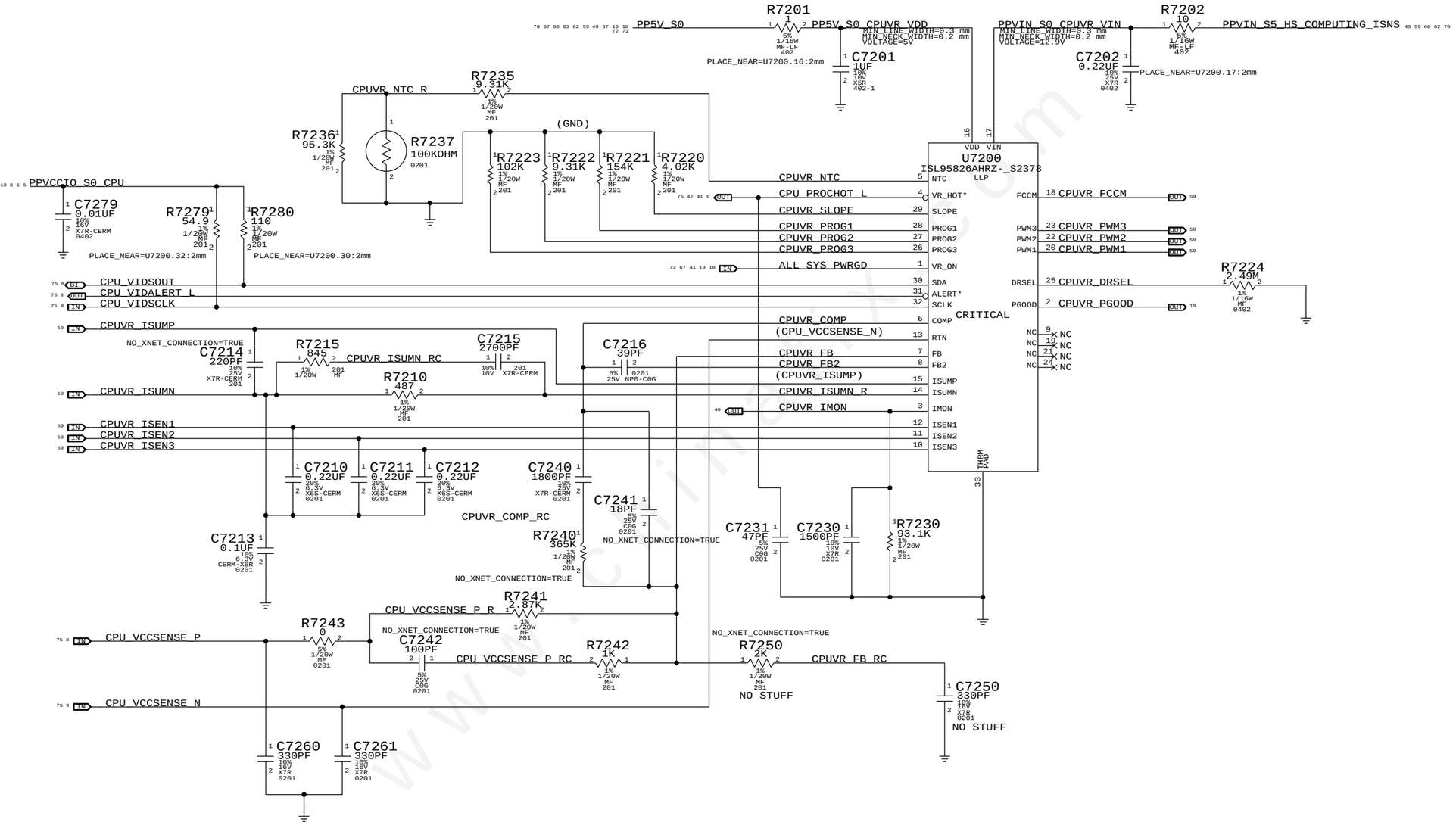

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/24/2014

PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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PP5V_S0
PPVIN_S5_HS_COMPUTING_ISNS

PHASE 1

U7310 FDMF6808N PQFN CRITICAL 353S3836

R7311 0 5% 1/10W MF-LF 402
C7311 0.22UF 10% 16V CERM 402
CPUVR_BOOT1_RC
CPUVR_BOOT1
CPUVR_PHASE1_K
CPUVR_PWM1
CPUVR_FCCM
C7310 1UF 10% 16V X6S-CERM 0402
VDRV
CGND
PGND
VIN
VSWH

L7310 0.36UH-20%-36A-0.001080HM CRITICAL
PIMS103T-SM 152S1538
CPUVR_PHASE1
MIN_LINE_WIDTH=1.5 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE
SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH1
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
CPUVR_ISNS1_P
CPUVR_ISNS1_N
R7310 0.00075 1% 1W MF 0612-1 CRITICAL
R7312 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUVR_PH1_SNUB
C7312 0.001UF 10% 50V X7R-CERM 0402 DIDT=TRUE NOSTUFF
R7314 3.9 1% 1/20W MF 201
R7315 1K 1% 1/20W MF 201
R7316 10K 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
CPUVR_ISEN1
CPUVR_ISUMP
R7317 10K 1% 1/20W MF 201
R7318 10K 1% 1/20W MF 201
CPUVR_ISNS2_N
CPUVR_ISNS3_N

C7313 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7314 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7315 10UF 20% 16V X6S-CERM 0603 NOSTUFF CRITICAL
C7316 10UF 20% 16V X6S-CERM 0603 NOSTUFF CRITICAL
C7317 1UF 10% 16V X6S-CERM 0402
C7318 0.001UF 10% 50V X7R-CERM 0402 THESE TWO CAPS ARE FOR EMC
C7319 0.001UF 10% 50V X7R-CERM 0402

Additonal Input Bulk Caps
C7370 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7371 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7372 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7373 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7374 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7375 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7376 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7377 15UF 20% 16V TANT SM CRITICAL
C7378 15UF 20% 16V TANT SM CRITICAL
C7379 15UF 20% 16V TANT SM CRITICAL
C7380 15UF 20% 16V TANT SM CRITICAL
C7381 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7382 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7383 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7384 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL

PHASE 2

U7320 FDMF6808N PQFN CRITICAL 353S3836

R7321 0 5% 1/10W MF-LF 402
C7321 0.22UF 10% 16V CERM 402
CPUVR_BOOT2_RC
CPUVR_BOOT2
CPUVR_PHASE2_K
CPUVR_PWM2
CPUVR_FCCM
C7320 1UF 10% 16V X6S-CERM 0402
VDRV
CGND
PGND
VIN
VSWH

L7320 0.36UH-20%-36A-0.001080HM CRITICAL
PIMS103T-SM 152S1538
CPUVR_PHASE2
MIN_LINE_WIDTH=1.5 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE
SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH2
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
CPUVR_ISNS2_P
CPUVR_ISNS2_N
R7320 0.00075 1% 1W MF 0612-1 CRITICAL
R7322 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUVR_PH2_SNUB
C7322 0.001UF 10% 50V X7R-CERM 0402 DIDT=TRUE NOSTUFF
R7324 3.9 1% 1/20W MF 201
R7325 1K 1% 1/20W MF 201
R7326 10K 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
CPUVR_ISEN2
CPUVR_ISUMP
R7327 10K 1% 1/20W MF 201
R7328 10K 1% 1/20W MF 201
CPUVR_ISNS1_N
CPUVR_ISNS3_N

C7323 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7324 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7325 10UF 20% 16V X6S-CERM 0603 NOSTUFF CRITICAL
C7326 10UF 20% 16V X6S-CERM 0603 NOSTUFF CRITICAL
C7327 1UF 10% 16V X6S-CERM 0402
C7328 0.001UF 10% 50V X7R-CERM 0402 THESE TWO CAPS ARE FOR EMC
C7329 0.001UF 10% 50V X7R-CERM 0402

PHASE 3

U7330 FDMF6808N PQFN CRITICAL 353S3836

R7331 0 5% 1/10W MF-LF 402
C7331 0.22UF 10% 16V CERM 402
CPUVR_BOOT3_RC
CPUVR_BOOT3
CPUVR_PHASE3_K
CPUVR_PWM3
CPUVR_FCCM
C7330 1UF 10% 16V X6S-CERM 0402
VDRV
CGND
PGND
VIN
VSWH

L7330 0.36UH-20%-36A-0.001080HM CRITICAL
PIMS103T-SM 152S1538
CPUVR_PHASE3
MIN_LINE_WIDTH=1.5 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE
SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
CPUVR_ISNS3_P
CPUVR_ISNS3_N
R7330 0.00075 1% 1W MF 0612-1 CRITICAL
R7332 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUVR_PH3_SNUB
C7332 0.001UF 10% 50V X7R-CERM 0402 DIDT=TRUE NOSTUFF
R7334 3.9 1% 1/20W MF 201
R7335 1K 1% 1/20W MF 201
R7336 10K 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
CPUVR_ISEN3
CPUVR_ISUMP
R7337 10K 1% 1/20W MF 201
R7338 10K 1% 1/20W MF 201
CPUVR_ISNS1_N
CPUVR_ISNS2_N

C7333 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7334 68UF 20% 16V POLY-TANT CASE-D2E-SM CRITICAL
C7335 10UF 20% 16V X6S-CERM 0603 NOSTUFF CRITICAL
C7336 10UF 20% 16V X6S-CERM 0603 NOSTUFF CRITICAL
C7337 1UF 10% 16V X6S-CERM 0402
C7338 0.001UF 10% 50V X7R-CERM 0402 THESE TWO CAPS ARE FOR EMC
C7339 0.001UF 10% 50V X7R-CERM 0402

PPVCC_S0_CPU

Vout = 1.85V max
95A max output
f = 450 kHz

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012
PAGE TITLE: CPU VR12.5 VCC Power Stage
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 73 OF 118
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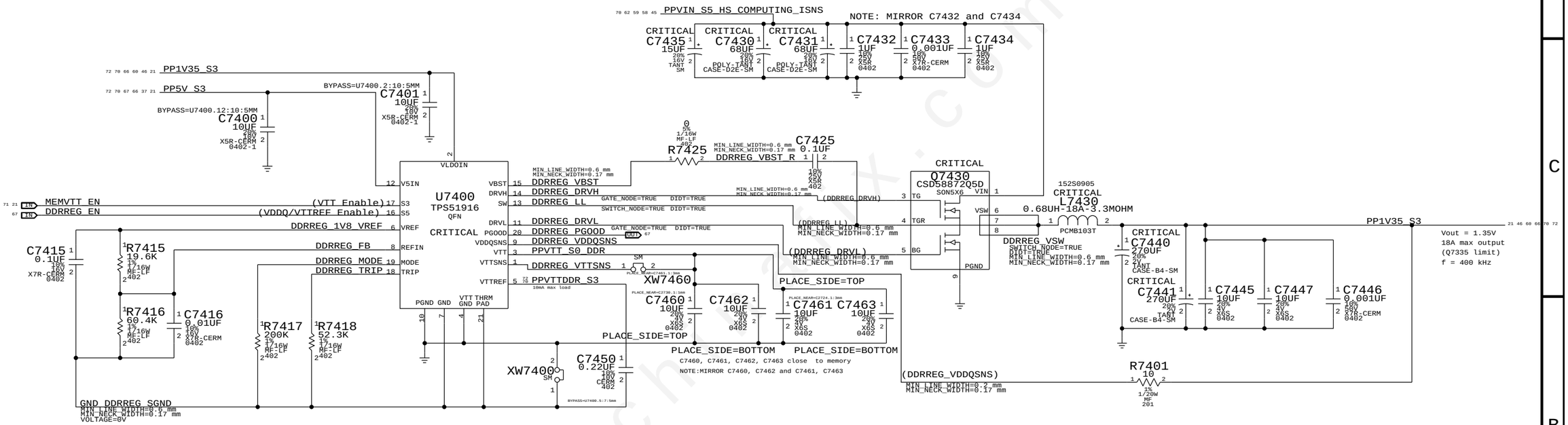
DDR3L (1V35 S3) REGULATOR



SYNC_MASTER=CLEAN_X305	SYNC_DATE=01/15/2014
PAGE TITLE	1.35V DDR3L SUPPLY
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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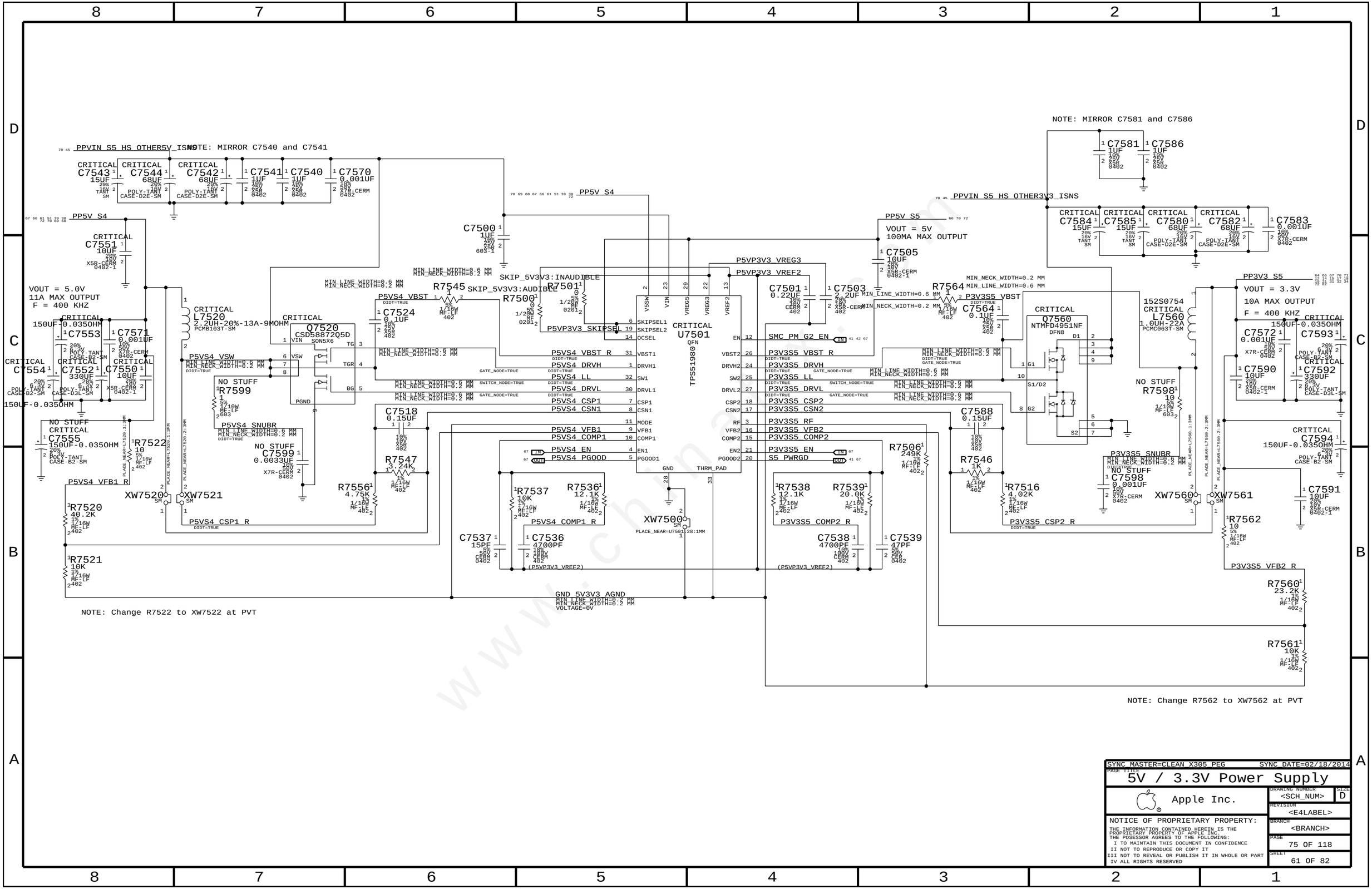
	SHEET 60 OF 82


PPVIN_S5_HS_OTHER5V_ISNS
NOTE: MIRROR C7540 and C7541
C7543 15UF 20% 16V TANT SM
C7544 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7542 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7541 1UF 10% 100V X5R 0402
C7540 1UF 10% 100V X5R 0402
C7570 0.001UF 10% 50V X7R-CERM 0402
PP5V_S4
C7551 10UF 20% 6.3V X5R-CERM 0402-1
VOUT = 5.0V
11A MAX OUTPUT
F = 400 KHZ
C7553 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
C7571 0.001UF 10% 50V X7R-CERM 0402
C7554 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
C7552 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7550 10UF 20% 6.3V X5R-CERM 0402-1
150UF-0.035OHM
NO STUFF
C7555 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
R7522 10 5% 1/16W MF-LF 402
PLACE_NEAR=L7520.1:3MM
P5VS4_VFB1_R
R7520 40.2K 1% 1/16W MF-LF 402
R7521 10K 1% 1/16W MF-LF 402
XW7520 SM
XW7521 SM
PLACE_NEAR=L7520.2:3MM
P5VS4_CSP1_R
DIDT=TRUE
L7520 2.2UH-20%-13A-9MOHM PCMB103T-SM
P5VS4_VSW
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
Q7520 CSD58872Q5D VIN SON5X6
TG
TGR
BG
PGND
NO STUFF
R7599 1 5% 1/10W MF-LF 603
P5VS4_SNUBR
NO STUFF
C7599 0.0033UF 10% 50V X7R-CERM 0402
C7518 0.15UF 10% 10V X5R 402
R7547 3.24K 1% 1/16W MF-LF 402
R7556 4.75K 1% 1/10W MF-LF 402
PP5V_S4
C7500 1UF 10% 25V X5R 603-1
SKIP_5V3V3:INAUDIBLE
SKIP_5V3V3:AUDIBLE
R7545 1 5% 1/10W MF-LF 402
R7500 0 5% 1/20W MF 0201
R7501 0 5% 1/20W MF 0201
P5VS4_VBST
C7524 0.1UF 10% 25V X5R 402
P5VP3V3_SKIPSEL
P5VP3V3_VREG3
P5VP3V3_VREF2
U7501 TPS51980 QFN
CRITICAL
SKIPSEL1
SKIPSEL2
OCSEL
VBST1
DRVH1
SW1
DRVL1
CSP1
CSN1
MODE
VFB1
COMP1
EN1
PGOOD1
P5VS4_VBST_R
P5VS4_DRVH
P5VS4_LL
P5VS4_DRVL
P5VS4_CSP1
P5VS4_CSN1
P5VS4_VFB1
P5VS4_COMP1
P5VS4_EN
P5VS4_PGOOD
GND
THRM_PAD
XW7500 SM
PLACE_NEAR=U7501.28:1MM
R7537 10K 1% 1/16W MF-LF 402
R7536 12.1K 1% 1/16W MF-LF 402
P5VS4_COMP1_R
C7537 15PF 5% 50V CERM 0402
C7536 4700PF 10% 100V CERM 402
(P5VP3V3_VREF2)
GND_5V3V3_AGND
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
NOTE: Change R7522 to XW7522 at PVT
PP5V_S5
VOUT = 5V
100MA MAX OUTPUT
C7505 10UF 20% 16V X5R-CERM 0402-1
C7501 0.22UF 10% 16V CERM 402
C7503 2.2UF 20% 10V X5R-CERM 402
SMC_PM_G2_EN
P3V3S5_VBST_R
P3V3S5_DRVH
P3V3S5_LL
P3V3S5_DRVL
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_EN
S5_PWRGD
R7506 249K 1% 1/16W MF-LF 402
C7588 0.15UF 10% 10V X5R 402
R7546 1K 1% 1/16W MF-LF 402
R7538 12.1K 1% 1/16W MF-LF 402
R7539 20.0K 1% 1/16W MF-LF 402
P3V3S5_COMP2_R
C7538 4700PF 10% 100V CERM 402
C7539 47PF 5% 50V CERM 0402
(P5VP3V3_VREF2)
R7564 1 5% 1/10W MF-LF 402
P3V3S5_VBST
C7564 0.1UF 10% 25V X5R 402
Q7560 NTMFD4951NF DFN8
R7516 4.02K 1% 1/16W MF-LF 402
P3V3S5_CSP2_R
DIDT=TRUE
NOTE: MIRROR C7581 and C7586
C7581 1UF 10% 25V X5R 0402
C7586 1UF 10% 25V X5R 0402
PPVIN_S5_HS_OTHER3V3_ISNS
C7584 15UF 20% 16V TANT SM
C7585 15UF 20% 16V TANT SM
C7580 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7582 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7583 0.001UF 10% 50V X7R-CERM 0402
PP3V3_S5
VOUT = 3.3V
10A MAX OUTPUT
F = 400 KHZ
152S0754
L7560 1.0UH-22A PCMC063T-SM
C7572 0.001UF 10% 50V X7R-CERM 0402
C7593 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
C7590 10UF 20% 6.3V X5R-CERM 0402-1
C7592 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7594 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B2-SM
NO STUFF
R7598 10 5% 1/10W MF-LF 603
P3V3S5_SNUBR
NO STUFF
C7598 0.001UF 10% 50V X7R-CERM 0402
C7591 10UF 20% 6.3V X5R-CERM 0402-1
XW7560 SM
XW7561 SM
PLACE_NEAR=L7560.1:3MM
PLACE_NEAR=L7560.2:3MM
R7562 10 5% 1/16W MF-LF 402
P3V3S5_VFB2_R
R7560 23.2K 1% 1/16W MF-LF 402
R7561 10K 1% 1/16W MF-LF 402
NOTE: Change R7562 to XW7562 at PVT
SYNC_MASTER=CLEAN_X305_PEG
SYNC_DATE=02/18/2014
PAGE TITLE
5V / 3.3V Power Supply
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 75 OF 118
SHEET 61 OF 82
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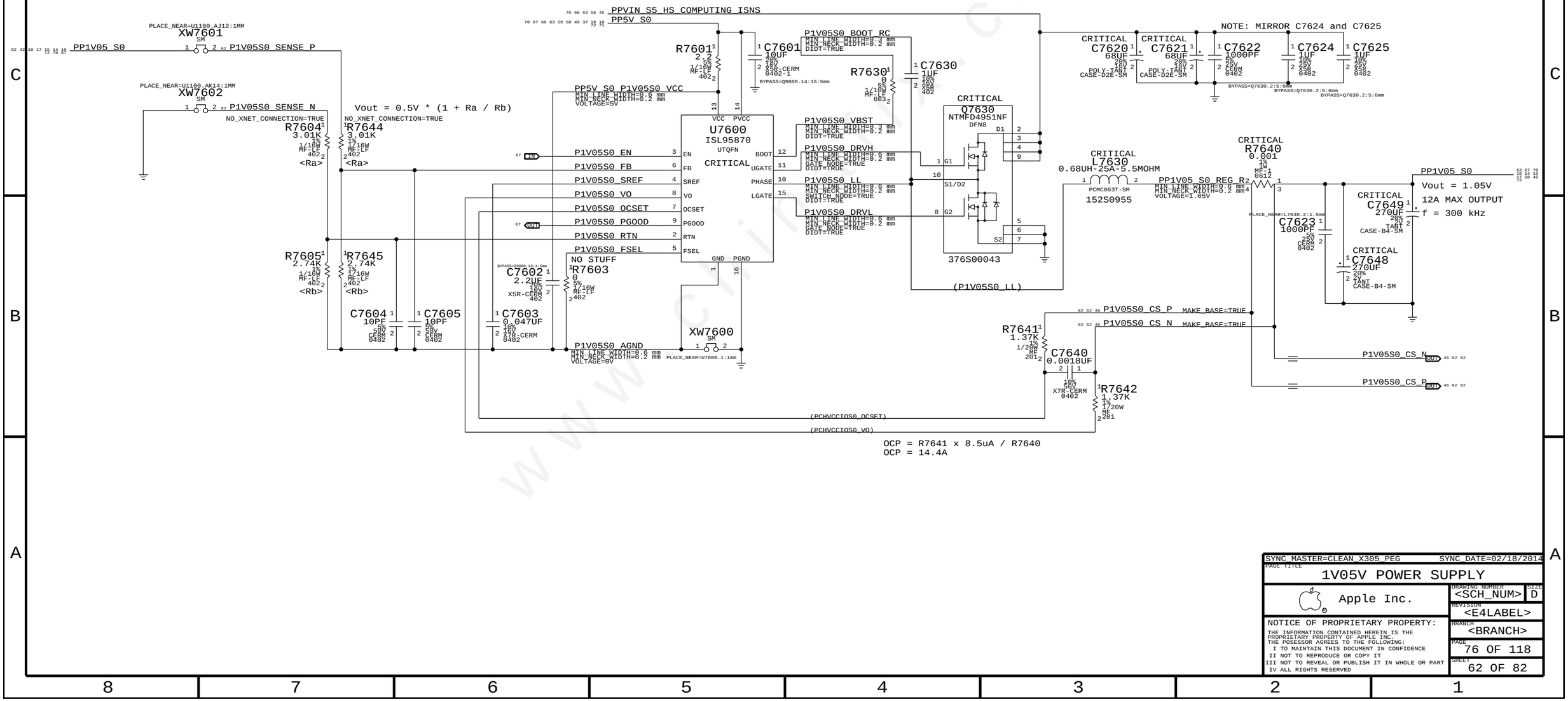
1V05 S0 REGULATOR



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: 1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 76 OF 118
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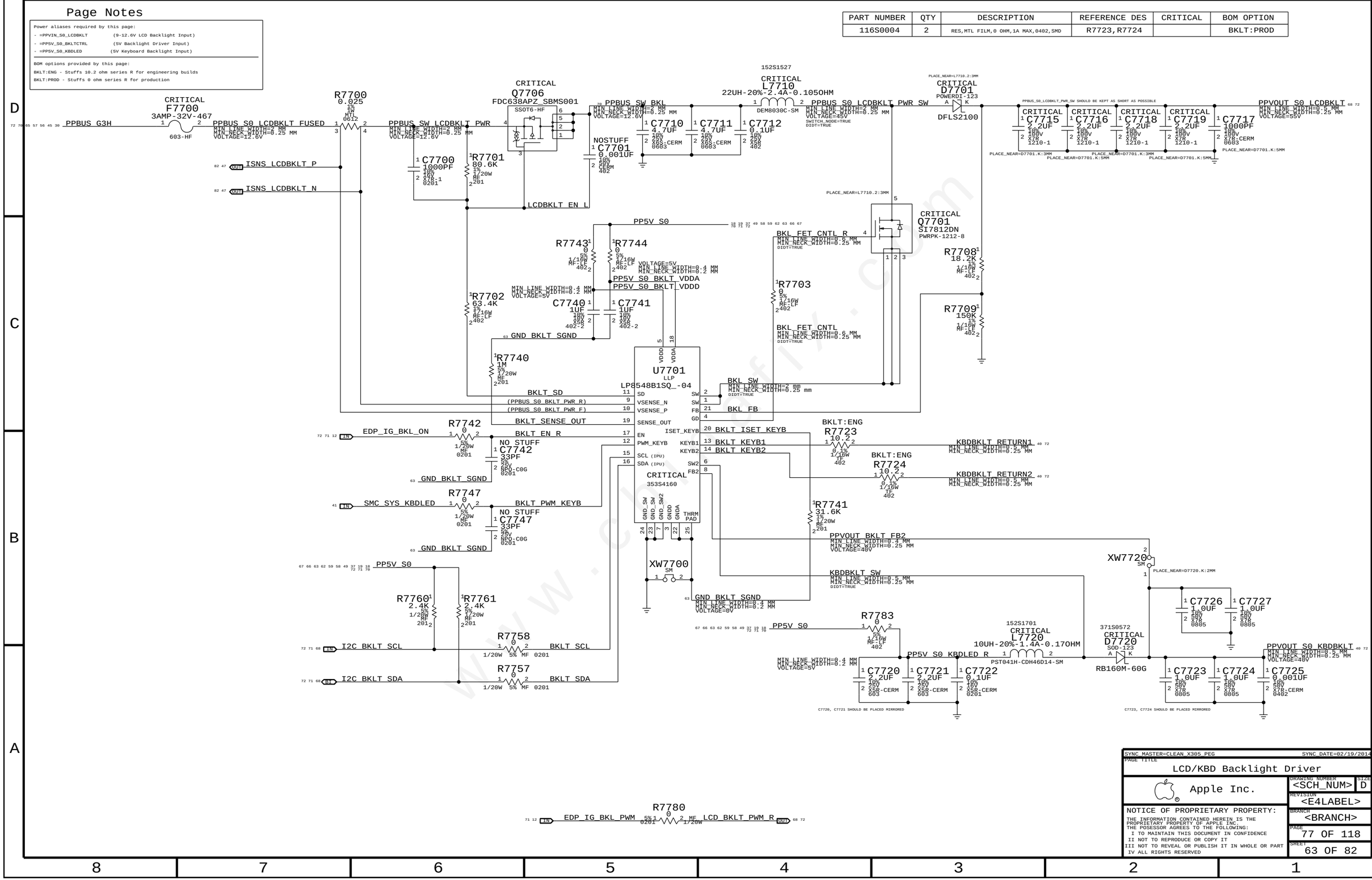
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7723,R7724		BKLT:PROD



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/19/2014

PAGE TITLE: LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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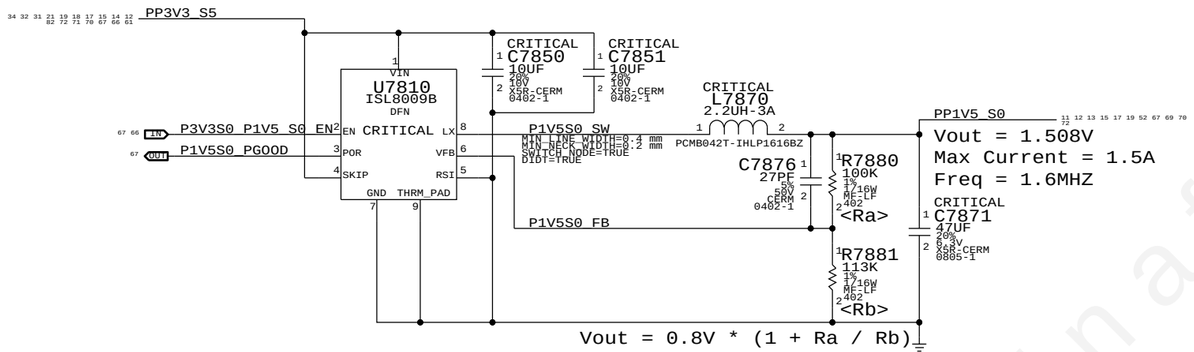
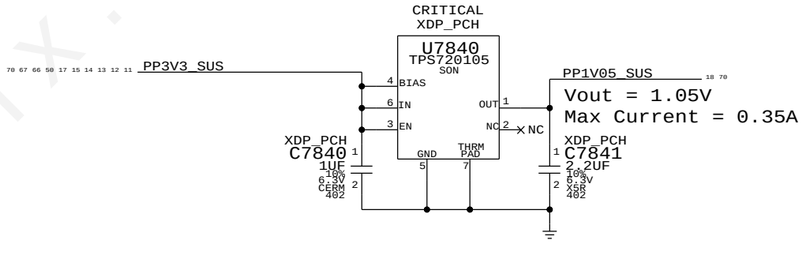
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC_MASTER=CLEAN X305 SYNC_DATE=01/15/2014

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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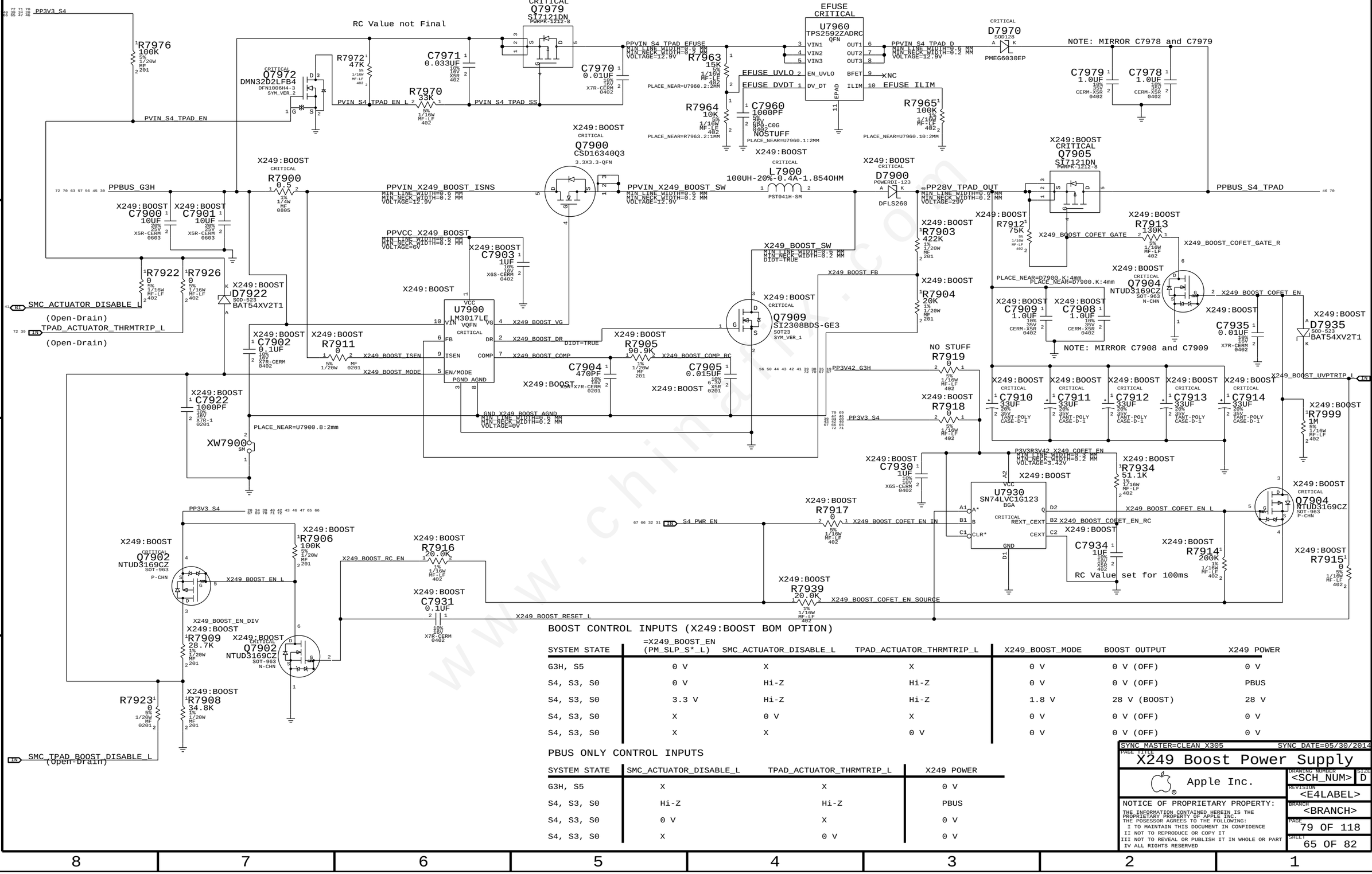


BOOST CONTROL INPUTS (X249:BOOST BOM OPTION)

SYSTEM STATE	=X249_BOOST_EN (PM_SLP_S*_L)	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	X249_BOOST_MODE	BOOST OUTPUT	X249 POWER
G3H, S5	0 V	X	X	0 V	0 V (OFF)	0 V
S4, S3, S0	0 V	Hi-Z	Hi-Z	0 V	0 V (OFF)	PBUS
S4, S3, S0	3.3 V	Hi-Z	Hi-Z	1.8 V	28 V (BOOST)	28 V
S4, S3, S0	X	0 V	X	0 V	0 V (OFF)	0 V
S4, S3, S0	X	X	0 V	0 V	0 V (OFF)	0 V

PBUS ONLY CONTROL INPUTS

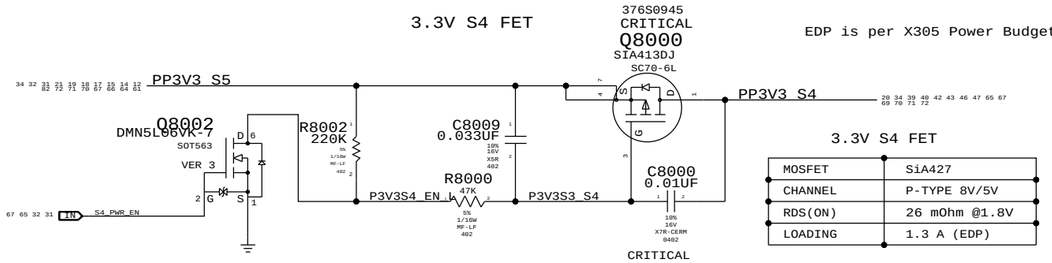
SYSTEM STATE	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	X249 POWER
G3H, S5	X	X	0 V
S4, S3, S0	Hi-Z	Hi-Z	PBUS
S4, S3, S0	0 V	X	0 V
S4, S3, S0	X	0 V	0 V

SYNC_MASTER=CLEAN X305 SYNC_DATE=05/30/2014

PAGE TITLE: X249 Boost Power Supply

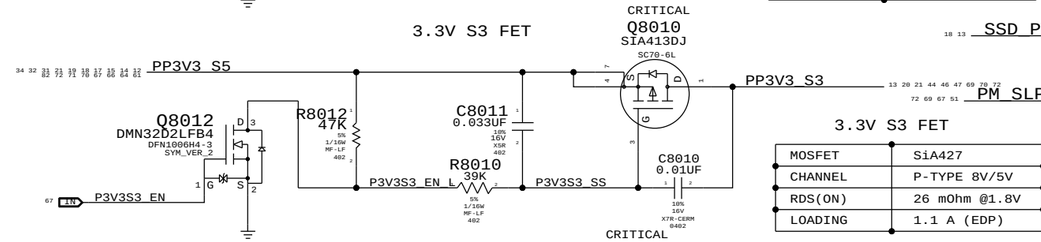
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 79 OF 118
SHEET: 65 OF 82

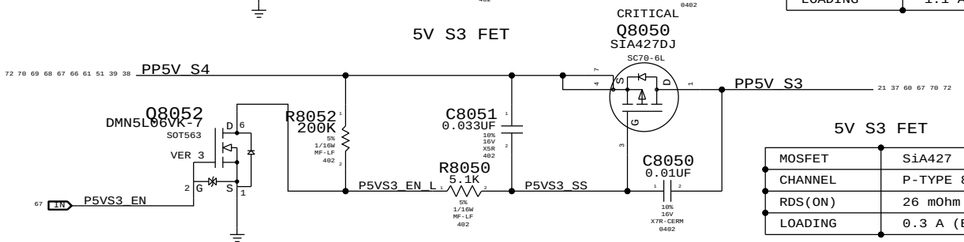


EDP is per X305 Power Budget rev??

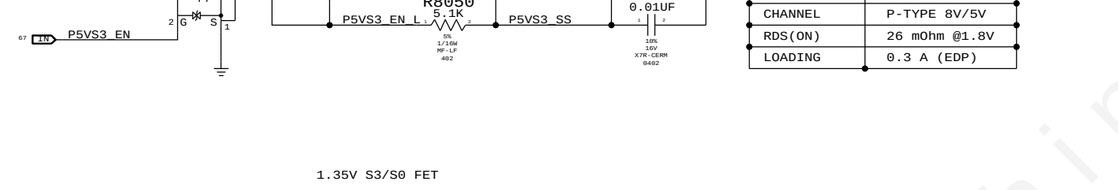
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)



3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

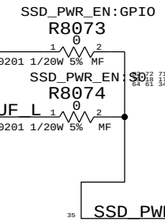


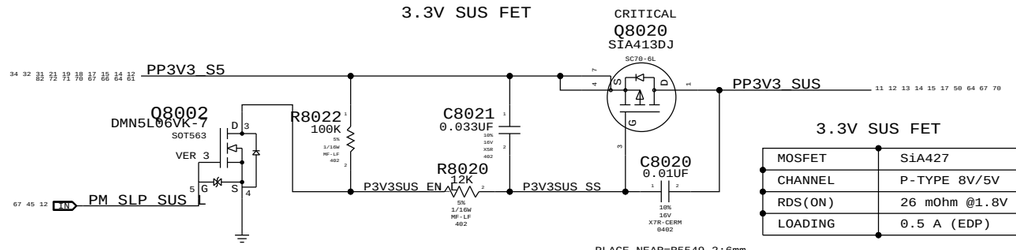
5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)



1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SSD_PWR_EN:GPIO

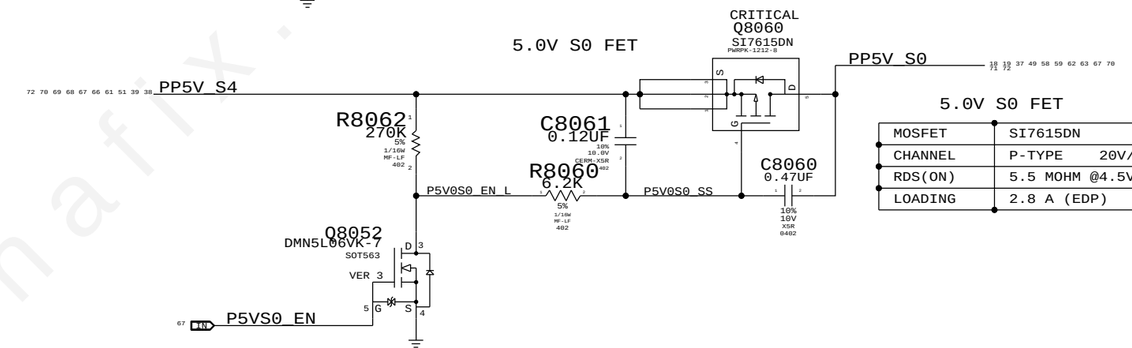




3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

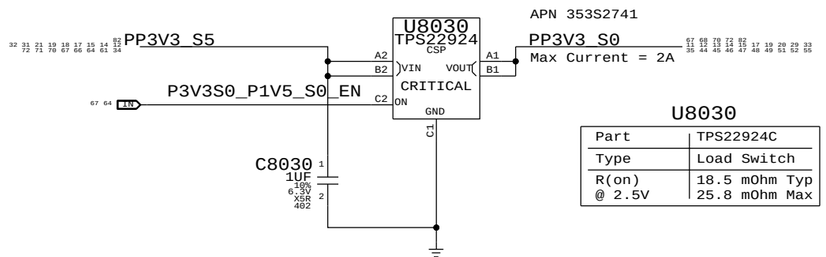
PLACE_NEAR=R5549.2:6mm

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 Switch



U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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Power State Debug LEDs
(For development only)

PP3V3_S5 → DBGLED R8194 0 (PLACE_SIDE=BOTTOM, MIN_NECK_WIDTH=0.1 MM, MIN_LINE_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED R8190 20K	DBGLED R8191 20K	DBGLED R8192 20K	DBGLED R8193 20K	5% 1/20W MF 201
DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0	
DBGLED D8190	DBGLED D8191	DBGLED D8192	DBGLED D8193	GREEN-56MCD-2MA-2.65V LTQH9G-SM
PLACE_SIDE=BOTTOM SILK_PART=S5_ON	PLACE_SIDE=BOTTOM SILK_PART=S4_ON	PLACE_SIDE=BOTTOM SILK_PART=S3_ON	PLACE_SIDE=BOTTOM SILK_PART=S0_ON	
DBGLED_S5_D Q8190 DMN5L06VK-7	DBGLED_S4_D Q8190 DMN5L06VK-7	DBGLED_S3_D Q8190 DMN5L06VK-7	DBGLED_S0_D Q8191 DMN32D2LFB4	SOT563 VER 3

S4_PWR_EN, PM_SLP_S4_L, PM_SLP_S3_BUF_L

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

PP3V3_S5 → C8170 0.1uF → PM_SLP_S5_L (PM_SLP_S5_L:100K pull down on PCH page)

SMC_S4_WAKESRC_EN, PM_SLP_S4_L → U8170 74LVC1G32 SOT891 → S4_PWR_EN (MAKE_BASE=TRUE)

S4_PWR_EN → S4 PWR EN ×4 (OUT)

S4_PWR_EN → D8174 BAT54XV2T1 SOD-523 → R8174 43K → P5VS4_EN (MAKE_BASE=TRUE)

P5VS4_EN_D → R8175 240 → C8174 2.2UF

S3 ENABLE

PM_SLP_S4_L (IN) (PM_SLP_S4_L:100K pull down in PCH page)

R8111 5.1K	R8112 0	R8113 0	R8114 3.3K
5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/20W MF 201
C8110 0.47UF	C8112 0.47UF	C8113 0.47UF	C8114 0.47UF
10% 6.3V CERM-X5R 402	10% 6.3V CERM-X5R 402	NO STUFF 10% 6.3V CERM-X5R 402	NO STUFF 10% 6.3V CERM-X5R 402

TPAD_VBUS_EN_R (OUT)

P5VS3_EN — P5VS3_EN (MAKE_BASE=TRUE)

P3V3S3_EN — P3V3S3_EN (MAKE_BASE=TRUE)

DDRREG_EN — DDRREG_EN (MAKE_BASE=TRUE)

S0 ENABLE

PP3V3_S5 → C8180 0.1uF

PM_SLP_S3_L:100K pull down in PCH page

PM_SLP_S3_L (IN) → R8178 100 → PM_SLP_S3_R_L (MAKE_BASE=TRUE)

MC74VHC1G08 SC70-HF → U8180

(PM_SLP_S3_BUF_L) → NO STUFF R8180 100K → D8185 SOD-523 BAT54XV2T1

P1V05_EN_D → R8138 820

R8185 130K	R8186 20K	R8187 0
5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402
C8185 0.82UF	C8186 0.68UF	C8187 0.68UF
10% 6.3V X5R 402	10% 6.3V CERM 402	10% 6.3V CERM 402 NO STUFF

PM_SLP_S3_BUF_L (OUT)

P5VS0_EN — P5VS0_EN (MAKE_BASE=TRUE)

P3V3S0_P1V5_S0_EN — P3V3S0_P1V5_S0_EN

P1V05S0_EN — P1V05S0_EN

PM_SLP_S3_R_L (OUT) ×2

CPUVCORE ENABLE

ALL_SYS_PWRGD — ALL_SYS_PWRGD (MAKE_BASE=TRUE) (OUT)

3.3V SUS Enable

PM_SLP_SUS_L (IN) — PM_SLP_SUS_L (MAKE_BASE=TRUE) (OUT) ×2

PM_SLP_SUS_L: 100K pull down on PCH page

S0 Rail PGOOD (BJT Version)

PP5V_S0 → R8151 54.9K → VMON_5V_DIV (5.0V Divider:1.07V) → R8152 15.0K

PP3V3_S5 → R8156 150K → S0PGD_C → ALL_SYS_PWRGD

R8153 1K VMON_Q2_BASE; R8154 1K NC / VMON_Q3_BASE; R8155 1K VMON_Q4_BASE

PP1V35_S3RS0_CPUDDR → R8154

PP3V3_S0 → R8158 15.0K → VMON_3V3_DIV (3V3 Divider:1.07V) → R8159 7.15K

Q8150 ASMCC0179 DFN2015H4-8 353S2809 (Q1 Q2 Q3 CRITICAL Q4)

S0PGD_BJT_GND_R → R8157 100

Vbe 0.7V max @2mA
Vce(sat) 0.1V max @1mA
Q1 Vth 0.7~1V @Id 250uA

3.3V SUS Detect

PP3V3_S5 → C8130 0.1uF

PP3V3_SUS → R8133 100K

U8130 TPS3808G33DBVRG4 SOT23-6 (CRITICAL)
SENSE, VDD, RESET*, CT, MR*, GND

PM_RSMRST_L (OUT) (PM_RSMRST_L goes to U1100.C21)

SUS_PGOOD_CT → C8131 0.001UF (NO STUFF)

TP_SUS_PGOOD_MR_L

S5 Rail Enables & PGOOD

PP3V42_G3H (PLACE_NEAR=U7501.20:7mm) → R8141 100K → S5_PWRGD-->SMC, SMC-->PM_DSW_PWRGD

SMC_PM_G2_EN (IN) (MAKE_BASE=TRUE) → R8140 100 → P3V3S5_EN — P3V3S5_EN (MAKE_BASE=TRUE) (OUT)

SMC_PM_G2_EN (OUT) → NO STUFF C8142 0.0033UF (PLACE_NEAR=U7501.21:7mm)

S5_PWRGD — S5_PWRGD (MAKE_BASE=TRUE) (OUT)

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

PP3V3_S4 → R8125 330K → PM_WLAN_EN (IN) — PM_WLAN_EN (MAKE_BASE=TRUE) (OUT)

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 0.915V-3.009V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

keep R8171 DDRCPU 1.35V only

PP3V3_S0 → C8162 0.1UF (NOSTUFF) → PP3V3_S0_VMON_P2 → R8195 10 → S0PGOOD_ISL

PP3V3_S0_VMON_P7 → C8161 0.1UF → S0PGOOD_ISL

PP3V3_S0 → C8163 0.1UF (NOSTUFF) → PP3V3_S0_VMON_P7 → R8196 10 → R8197 100K (NOSTUFF)

PP5V_S0 → PP1V35_S3RS0_CPUDDR

R8160 6.04K; R8170 10K; R8172 6.04K; R8161 15.0K; R8171 12.4K; R8173 15.0K

PSV_VMON divider 3.16V @4.5V
1V35_VMON divider 0.731V @1.31V
1V05_VMON divider 0.716V @1.02V

U8160 ISL88042IRTEZ TDFN (CRITICAL)
VDD, V2MON, V3MON, V4MON, RST*, GND, THRM_PAD

S0PGOOD_ISL → R8162 1K → PM_SLP_S3_BUF_L

R8167 10K → P1V5S0_PGOOD (OUT)

R8168 100 → P1V05S0_PGOOD (OUT)

R8169 100 → DDRREG_PGOOD (OUT)

R8120 100 → DDRREG_PGOOD:Y

R8162 330 → ALL_SYS_PWRGD

1V5 S0 "PGOOD" Delay

PP3V3_S5 → R8136 23.7K → PM_1V5_PGD_L → R8139 2.0K → PM_1V5_PGD_L_R

C8134 2.2UF

CRITICAL Q8151 DMB53D0UV SOT-563 (Vgs:0.7V~1.0V)

PP1V5_S0 → R8135 54.9K → PM_1V5_PGD_DIV → R8134 61.9K

CRITICAL Q8151 DMB53D0UV SOT-563

VBEon: 0.58~0.7V
1V5 Divider:0.75~0.85V

R8137 100 DELAY_1V5S0_PGD → ALL_SYS_PWRGD (OUT)

CHGR VFRQ Generation

VFRQ High: Variable Frequency
VFRQ Low: Fix Frequency

PP3V42_G3H → R8131 100K → CHGR_VFRQ (OUT)

Unused PGOOD signals

Q8131 DMN32D2LFB4 SYM_VER_2

PP5V_S3 → DDRREG_PGOOD:N → R8166 470K → PP5V_S4 → R8165 470K

DDRREG_PGOOD (IN)

P5VS4_PGOOD (IN)

PM_SLP_S3_R_L

SYNC_MASTER=CLEAN_X305	SYNC_DATE=05/30/2014
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER <SCH_NUM> D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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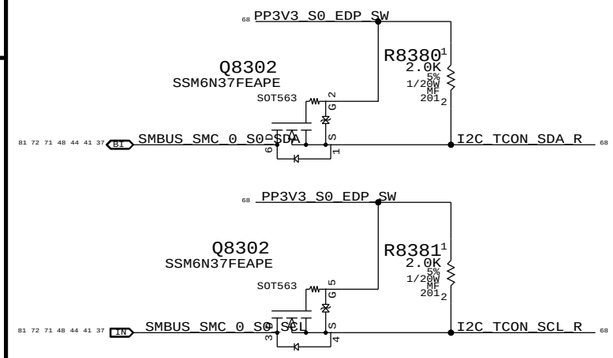
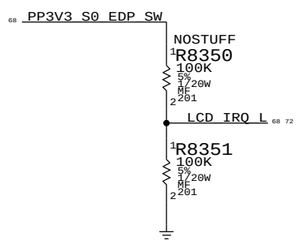
	SHEET 67 OF 82

LCD PANEL INTERFACE (eDP)



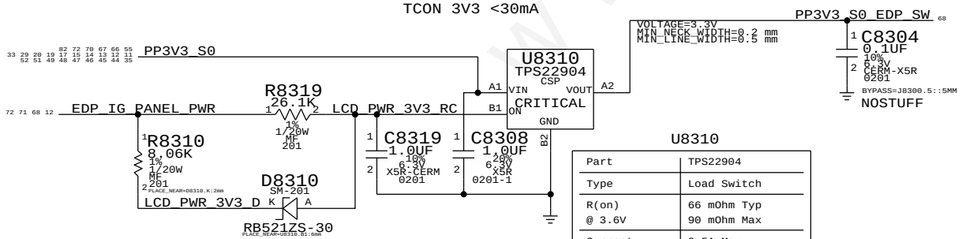


U8300

Part	SLG5AP1443V
Type	Load Switch
R(on) @100mA	17 mOhm Typ 19 mOhm Max
Current	2.5 A Max

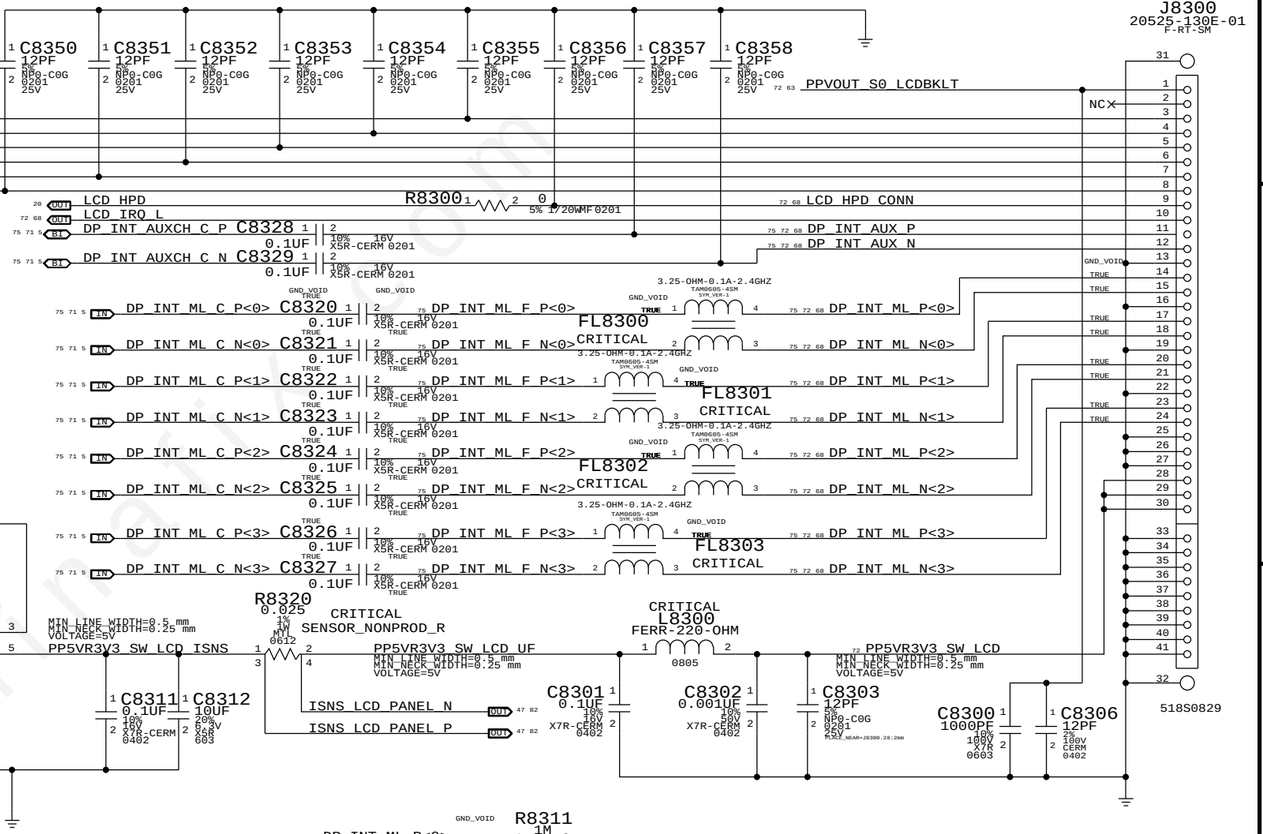
3.3V TCON Switch

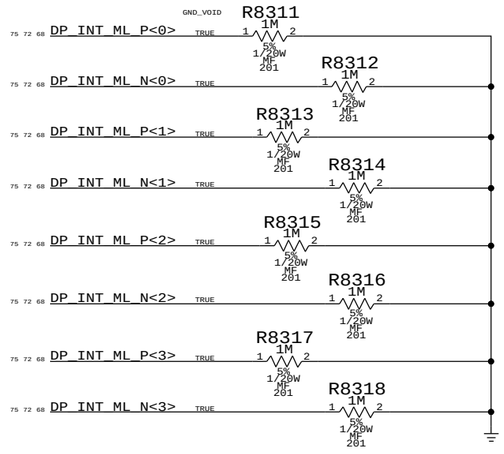
TCON 3V3 <30mA



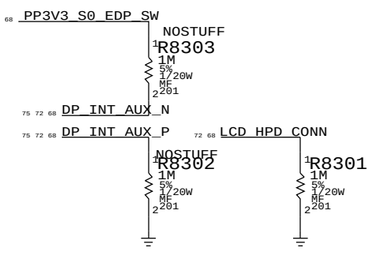
U8310

Part	TPS22904
Type	Load Switch
R(on) @ 3.6V	66 mOhm Typ 90 mOhm Max
Current	0.5A Max





LCD Panel HPD & AUX strapping



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/10/2014

PAGE TITLE

eDP Display Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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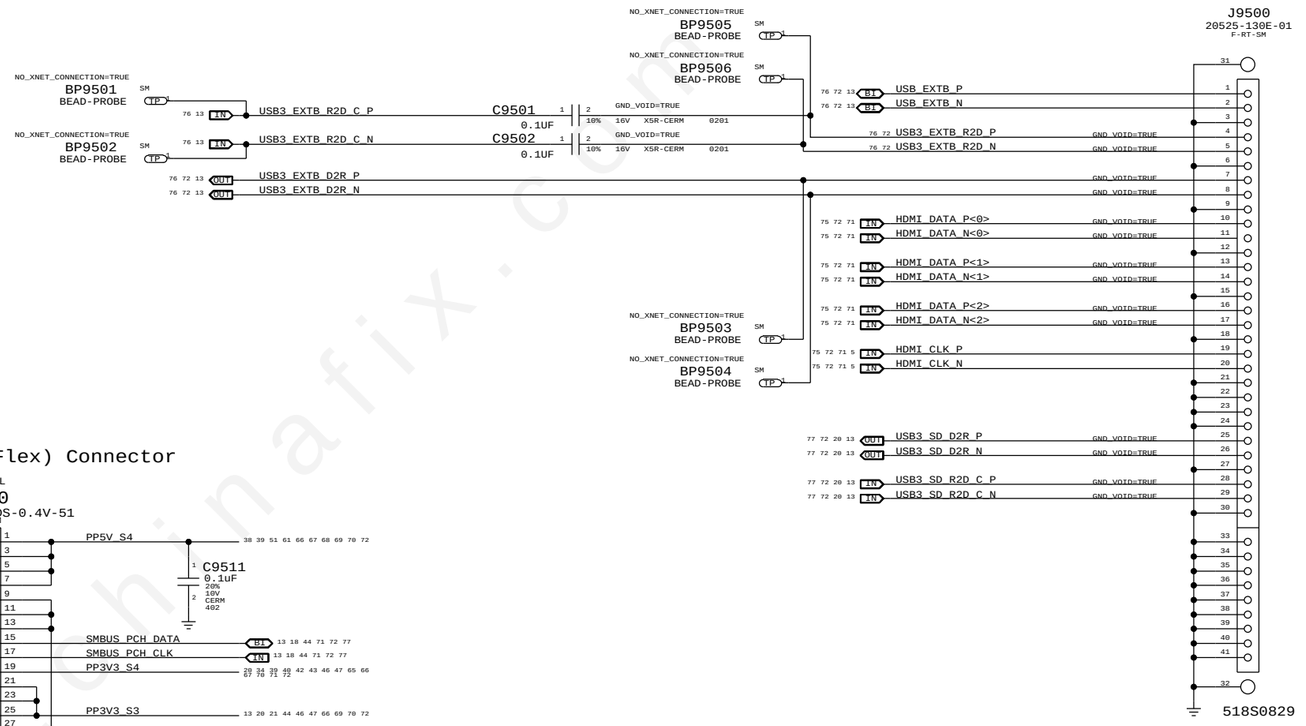
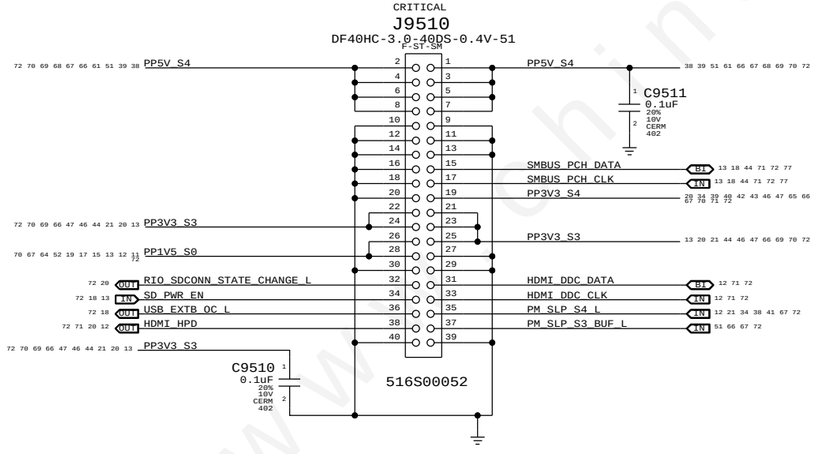
Wire-to-Board (Micro-coax) Connector



Board-to-Board (Flex) Connector



SYNC_MASTER=CLEAN_X305G SYNC_DATE=01/14/2014

PAGE TITLE: RIO Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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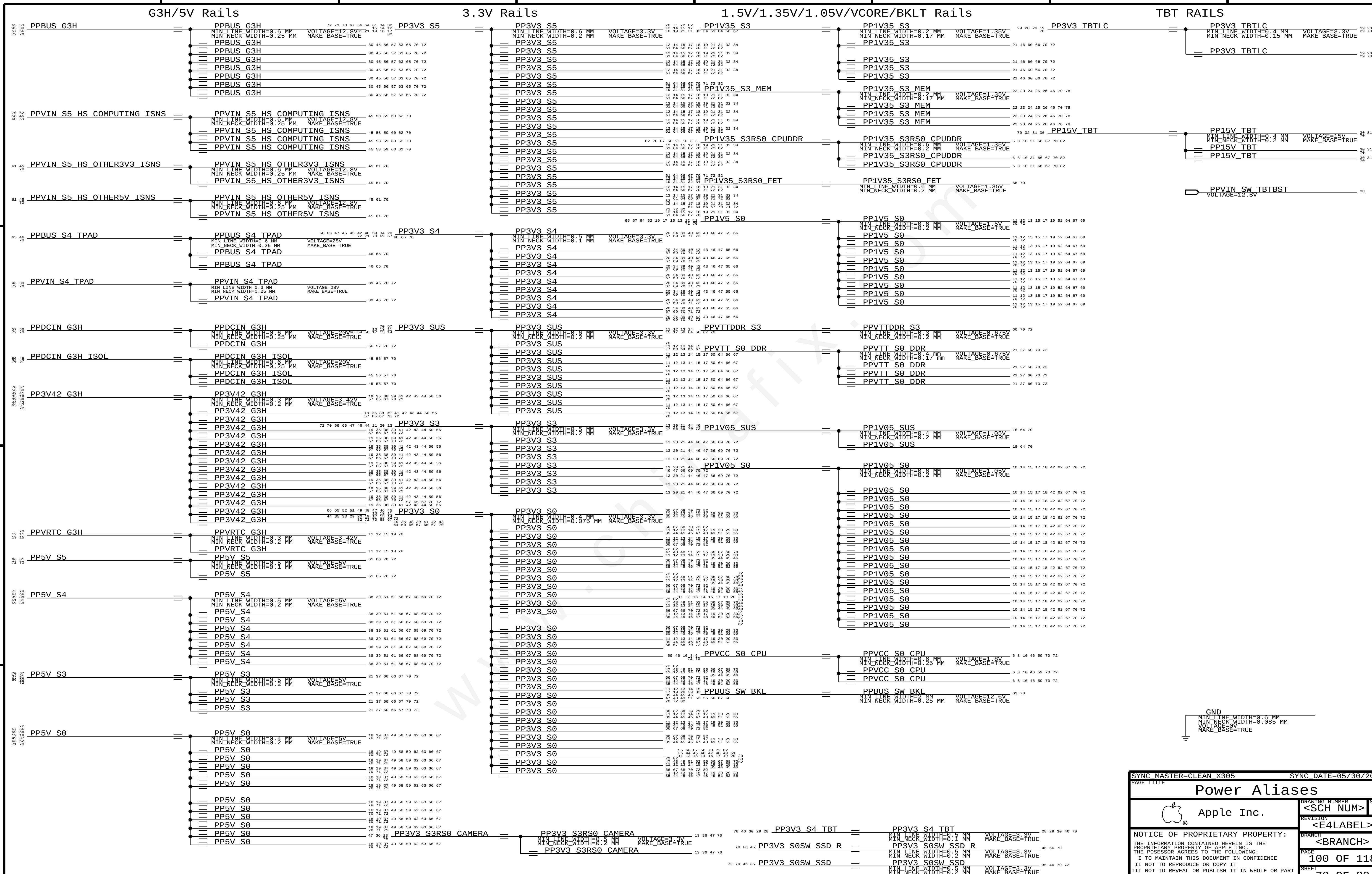

SYNC_MASTER=CLEAN_X305 SYNC_DATE=05/30/2014

PAGE TITLE

Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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Display Aliases

72 71 68 12	EDP_IG_PANEL_PWR	MAKE_BASE=TRUE	EDP_IG_PANEL_PWR	12 68 71 72
72 71 63 12	EDP_IG_BKL_ON	MAKE_BASE=TRUE	EDP_IG_BKL_ON	12 63 71 72
71 63 12	EDP_IG_BKL_PWM	MAKE_BASE=TRUE	EDP_IG_BKL_PWM	12 63 71
75 68 5	DP_INT_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLP<3..0>	
75 68 5	DP_INT_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLN<3..0>	
75 71 68 5	DP_INT_AUXCH_C_P	MAKE_BASE=TRUE	DP_INT_AUXCH_C_P	5 68 71 75
75 71 68 5	DP_INT_AUXCH_C_N	MAKE_BASE=TRUE	DP_INT_AUXCH_C_N	5 68 71 75
71 28 12	DP_TBTSNK0_HPD	MAKE_BASE=TRUE	DP_TBTSNK0_HPD	12 28 71
75 28 5	DP_TBTSNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLP<3..0>	
75 28 5	DP_TBTSNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLN<3..0>	
75 71 28 12	DP_TBTSNK0_AUXCH_C_P	MAKE_BASE=TRUE	DP_TBTSNK0_AUXCH_C_P	12 28 71 75
75 71 28 12	DP_TBTSNK0_AUXCH_C_N	MAKE_BASE=TRUE	DP_TBTSNK0_AUXCH_C_N	12 28 71 75
71 33 12	DP_TBTSNK0_DDC_DATA	MAKE_BASE=TRUE	DP_TBTSNK0_DDC_DATA	12 33 71
71 33 12	DP_TBTSNK0_DDC_CLK	MAKE_BASE=TRUE	DP_TBTSNK0_DDC_CLK	12 33 71
71 28 12	DP_TBTSNK1_HPD	MAKE_BASE=TRUE	DP_TBTSNK1_HPD	12 28 71
75 28 5	DP_TBTSNK1_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLP<3..0>	
75 28 5	DP_TBTSNK1_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLN<3..0>	
75 71 28 12	DP_TBTSNK1_AUXCH_C_P	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_P	12 28 71 75
75 71 28 12	DP_TBTSNK1_AUXCH_C_N	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_N	12 28 71 75
71 33 12	DP_TBTSNK1_DDC_DATA	MAKE_BASE=TRUE	DP_TBTSNK1_DDC_DATA	12 33 71
71 33 12	DP_TBTSNK1_DDC_CLK	MAKE_BASE=TRUE	DP_TBTSNK1_DDC_CLK	12 33 71
72 71 69 20 12	HDMI_HPD	MAKE_BASE=TRUE	HDMI_HPD	12 20 69 71 72
75 72 69	HDMI_DATA_P<0..2>	MAKE_BASE=TRUE	TP_DP_IG_D_MLP<2..0>	5
75 72 69	HDMI_DATA_N<0..2>	MAKE_BASE=TRUE	TP_DP_IG_D_MLN<2..0>	5
75 72 71 69 5	HDMI_CLK_P	MAKE_BASE=TRUE	HDMI_CLK_P	5 69 71 72 75
75 72 71 69 5	HDMI_CLK_N	MAKE_BASE=TRUE	HDMI_CLK_N	5 69 71 72 75
72 71 69 12	HDMI_DDC_CLK	MAKE_BASE=TRUE	HDMI_DDC_CLK	12 69 71 72
72 71 69 12	HDMI_DDC_DATA	MAKE_BASE=TRUE	HDMI_DDC_DATA	12 69 71 72

Unused TPAD SPI

66 65 47 46 43 42 40 39 34 20 72 71 70 69 67 PP3V3_S4

RA294 100K 1% 1/20W MF 201
RA295 100K 1% 1/20W MF 201
RA296 100K 1% 1/20W MF 201
RA297 100K 1% 1/20W MF 201
RA298 100K 1% 1/20W MF 201
RA299 100K 1% 1/20W MF 201

72 71 39	TPAD_SPI_BUS_EN 71 39	MAKE_BASE=TRUE	TPAD_SPI_BUS_EN 72 39	
77 72 71 39	TPAD_SPI_CS_L 72 71 39	MAKE_BASE=TRUE	TPAD_SPI_CS_L 74 39	
72 71 39	TPAD_SPI_INT_L 72 71 39	MAKE_BASE=TRUE	TPAD_SPI_INT_L	
77 72 71 39	TPAD_SPI_MISO 72 71 39	MAKE_BASE=TRUE	TPAD_SPI_MISO 74 39	
77 72 71 39	TPAD_SPI_MOSI 72 71 39	MAKE_BASE=TRUE	TPAD_SPI_MOSI 74 39	
77 72 71 39	TPAD_SPI_SCLK 72 71 39	MAKE_BASE=TRUE	TPAD_SPI_SCLK 74 39	

78 75 71 24 23 22	PP0V75_S3_MEM_VREFDQ_A	0.675V	MAKE_BASE=TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 71 75 78
75 71 26 25 22	PP0V75_S3_MEM_VREFDQ_B	0.675V	MAKE_BASE=TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 71 75
78 75 71 26 25 24 23 22	PP0V75_S3_MEM_VREFCA	0.675V	MAKE_BASE=TRUE	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 71 75 78
78 75 71 26 25 24 23 22	PP0V75_S3_MEM_VREFCA				
78 75 71 26 25 24 23 22	PP0V75_S3_MEM_VREFCA				

EDP CABLE

72 71 68 63	I2C_BKLT_SCL	MAKE_BASE=TRUE	I2C_BKLT_SCL	63 68 71 72
72 71 68 63	I2C_BKLT_SDA	MAKE_BASE=TRUE	I2C_BKLT_SDA	63 68 71 72
81 72 71 68 48 44 41 37	SMBUS_SMC_0_S0_SCL		SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72 81
81 72 71 68 48 44 41 37	SMBUS_SMC_0_S0_SDA		SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72 81

CPU signals

71 60 21 MEMVTT_EN — MEMVTT_EN 21 60 71 (MAKE_BASE=TRUE)

J9510 RIO FLEX CONN

77 72 71 69 44 18 13	SMBUS_PCH_DATA	SMBUS_PCH_DATA	13 18 44 69 71 72 77
77 72 71 69 44 18 13	SMBUS_PCH_CLK	SMBUS_PCH_CLK	13 18 44 69 71 72 77

SSD Signals Through PEG

75 35 5	PCIE_SSD_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<3..0>	OUT
75 35 5	PCIE_SSD_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<3..0>	OUT
75 35 5	PCIE_SSD_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<3..0>	IN
75 35 5	PCIE_SSD_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<3..0>	IN

Thunderbolt Signals Through PEG

75 28 5	PCIE_TBT_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<11..8>	OUT
75 28 5	PCIE_TBT_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<11..8>	OUT
75 28 5	PCIE_TBT_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<11..8>	IN
75 28 5	PCIE_TBT_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<11..8>	IN

Unused PEG Lanes

TP_PEG_D2RP<7..4>	MAKE_BASE=TRUE	=PEG_D2R_P<7..4>	5
TP_PEG_D2RN<7..4>	MAKE_BASE=TRUE	=PEG_D2R_N<7..4>	5
TP_PEG_R2D_CP<7..4>	MAKE_BASE=TRUE	=PEG_R2D_C_P<7..4>	5
TP_PEG_R2D_CN<7..4>	MAKE_BASE=TRUE	=PEG_R2D_C_N<7..4>	5
5 TP_PEG_D2RP<15..12>	MAKE_BASE=TRUE	=PEG_D2R_P<15..12>	
5 TP_PEG_D2RN<15..12>	MAKE_BASE=TRUE	=PEG_D2R_N<15..12>	
5 TP_PEG_R2D_CP<15..12>	MAKE_BASE=TRUE	=PEG_R2D_C_P<15..12>	
5 TP_PEG_R2D_CN<15..12>	MAKE_BASE=TRUE	=PEG_R2D_C_N<15..12>	

Unused PCH PCIE Lanes

	MAKE_BASE	NO_TEST	
13 NC_PCIE_SSD_D2RP<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_P<3..0>
13 NC_PCIE_SSD_D2RN<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_N<3..0>
13 NC_PCIE_SSD_R2D_CP<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_P<3..0>
13 NC_PCIE_SSD_R2D_CN<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_N<3..0>

71 49 PP3V3_S3_FAN_CTL — PP3V3_S3_FAN_CTL 49 71
(MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)

RA201 0 5% 1/20W MF 0201 — PP3V3_S5 12 14 15 17 18 19 21 31 32 34 61 64 66 67 70 72 82
RA202 0 5% 1/20W MF 0201 NOSTUFF — PP3V3_S4 20 34 39 40 42 43 46 47 65 66 67 69 70 71 72

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
14	DPMUX_UC_IRQ
14	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L
14	LPCPLUS_GPIO

67 66 63 62 59 58 49 37 19 18 72 70 PP5V_S0

XWA202 SM — PP5V_S0_AUDIO_AMP_L 53
XWA203 SM — PP5V_S0_AUDIO_AMP_R 53
(MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V)

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

Apple Inc.

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Functional Test Points

J3501 - airport

FUNC_TEST	AP_CLKREQ_Q_L	34
TRUE	AP_RESET_CONN_L	34
TRUE	PCIE_AP_D2R_PI_N	34 77
TRUE	PCIE_AP_D2R_PI_P	34 77
TRUE	PCIE_AP_R2D_N	34 77
TRUE	PCIE_AP_R2D_P	34 77
TRUE	PCIE_CLK100M_AP_CONN_N	34 77
TRUE	PCIE_CLK100M_AP_CONN_P	34 77
TRUE	PCIE_WAKE_L	12 34 36 77
TRUE	PP3V3_S3RS4_BT_F	34
TRUE	PP3V3_WLAN	34 42
TRUE	USB_BT_CONN_N	34 76
TRUE	USB_BT_CONN_P	34 76
TRUE	WIFI_EVENT_L	34 41 42
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	37 80
TRUE	MIPI_CLK_CONN_P	37 80
TRUE	CAM_SENSOR_WAKE_L_CONN	37
TRUE	MIPI_DATA_CONN_N	37 80
TRUE	MIPI_DATA_CONN_P	37 80
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72 81
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72 81
TRUE	I2C_CAM_SCK	36 37
TRUE	I2C_CAM_SDA	36 37
TRUE	PP5V_S3RS0_ALSCAM_F	37
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	5 69 71 75
TRUE	HDMI_CLK_P	5 69 71 75
TRUE	HDMI_DATA_N<0>	69 71 75
TRUE	HDMI_DATA_N<1>	69 71 75
TRUE	HDMI_DATA_N<2>	69 71 75
TRUE	HDMI_DATA_P<0>	69 71 75
TRUE	HDMI_DATA_P<1>	69 71 75
TRUE	HDMI_DATA_P<2>	69 71 75
TRUE	USB3_SD_D2R_N	13 20 69 77
TRUE	USB3_SD_D2R_P	13 20 69 77
TRUE	USB3_SD_R2D_C_N	13 20 69 77
TRUE	USB3_SD_R2D_C_P	13 20 69 77
TRUE	USB3_EXTB_D2R_N	13 69 76
TRUE	USB3_EXTB_D2R_P	13 69 76
TRUE	USB3_EXTB_R2D_N	69 76
TRUE	USB3_EXTB_R2D_P	69 76
TRUE	USB_EXTB_N	13 69 76
TRUE	USB_EXTB_P	13 69 76
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 69
TRUE	HDMI_DDC_CLK	12 69 71
TRUE	HDMI_DDC_DATA	12 69 71
TRUE	HDMI_HPD	12 20 69 71
TRUE	SMBUS_PCH_CLK	13 18 44 69 71 77
TRUE	SMBUS_PCH_DATA	13 18 44 69 71 77
TRUE	PM_SLP_S3_BUF_L	51 66 67 69
TRUE	PM_SLP_S4_L	12 21 34 38 41 67 69
TRUE	PP3V3_S3	3X 13 20 21 44 46 47 66 69 70 72
TRUE	PP3V3_S4	20 34 39 40 42 43 46 47 65 66 67 69 70 71 72
TRUE	PP5V_S4	5X 38 39 51 61 66 67 68 69 70 72
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 69
TRUE	USB_EXTB_OC_L	18 69
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	SMC_LID_R	43
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 58 59 62 63 66 67 70 71 72
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 58 59 62 63 66 67 70 71 72
TRUE	GND	5X

J6100 - spi

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	SMC_RESET_L	41 42 50 57
TRUE	SMC_TCK	41 42 50
TRUE	SMC_TMS	41 42 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	SPI_ALT_CLK	50 77
TRUE	SPI_ALT_CS_L	50 77
TRUE	SPI_ALT_IO0_MOSI	50 77
TRUE	SPI_ALT_IO1_MISO	50 77
TRUE	SPI_ALT_IO2_WP_L	50 77
TRUE	SPI_ALT_IO1_HOLD_L	50 77
TRUE	GND	2X

J4801 - ipd flex

TRUE	TPAD_SPI_INT_L	39 71
TRUE	TPAD_SPI_CS_L	39 71 77
TRUE	TPAD_SPI_MOSI	39 71 77
TRUE	TPAD_SPI_MISO	39 71 77
TRUE	TPAD_SPI_SCLK	39 71 77
TRUE	TPAD_SPI_BUS_EN	39 71
TRUE	USB_TPAD_N	13 39 76
TRUE	USB_TPAD_P	13 39 76
TRUE	IOXP2_INT_L	39
TRUE	I2C_IOXP_SCL	39
TRUE	I2C_IOXP_SDA	39
TRUE	SMC_PME_S4_WAKE_L	34 39 41 43
TRUE	TPAD_ACTUATOR_THRMTRIP_L	39 65
TRUE	TPAD_VBUS_EN	39
TRUE	SMBUS_SMC_2_S3_SCL	39 41 44 81
TRUE	SMBUS_SMC_2_S3_SDA	39 41 44 81
TRUE	SMC_LID	39 41 42 43
TRUE	SMC_ACTUATOR_EN_L	39 41
TRUE	PPVIN_S4_TPAD	4X 39 46 70
TRUE	GND_ACTUATOR	4X 39
TRUE	PP3V3_S4	20 34 39 40 42 43 46 47 65 66 67 69 70 71 72
TRUE	PP5V_S4	38 39 51 61 66 67 68 69 70 72
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 34 39 40 42 43 46 47 65 66 67 69 70 71 72
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	WS_CONTROL_KBD	39
TRUE	WS_KBD1	39
TRUE	WS_KBD10	39
TRUE	WS_KBD11	39
TRUE	WS_KBD12	39
TRUE	WS_KBD13	39
TRUE	WS_KBD14	39
TRUE	WS_KBD15_CAP	39
TRUE	WS_KBD16_NUM	39
TRUE	WS_KBD17	39
TRUE	WS_KBD18	39
TRUE	WS_KBD19	39
TRUE	WS_KBD2	39
TRUE	WS_KBD20	39
TRUE	WS_KBD21	39
TRUE	WS_KBD22	39
TRUE	WS_KBD23	39
TRUE	WS_KBD3	39
TRUE	WS_KBD4	39
TRUE	WS_KBD5	39
TRUE	WS_KBD6	39
TRUE	WS_KBD7	39
TRUE	WS_KBD8	39
TRUE	WS_KBD9	39
TRUE	WS_KBD_ONOFF_L	39
TRUE	WS_LEFT_OPTION_KBD	39
TRUE	WS_LEFT_SHIFT_KBD	39
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 40 63
TRUE	KBDBKLT_RETURN2	2X 40 63
TRUE	PPVOUT_S0_KBDBKLT	40 63
TRUE	GND	4X

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	66 67 68 70 72 82 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 82
TRUE	SPKRCONN_L_OUT_P	53 55 82
TRUE	SPKRCONN_SL_OUT_N	53 55 82
TRUE	SPKRCONN_SL_OUT_P	53 55 82
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 82
TRUE	SPKRCONN_R_OUT_P	53 55 82
TRUE	SPKRCONN_SR_OUT_N	53 55 82
TRUE	SPKRCONN_SR_OUT_P	53 55 82
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	41 44 56 57 81
TRUE	SMBUS_SMC_5_G3_SDA	41 44 56 57 81
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	68 75
TRUE	DP_INT_AUX_P	68 75
TRUE	DP_INT_ML_N<0>	68 75
TRUE	DP_INT_ML_N<1>	68 75
TRUE	DP_INT_ML_N<2>	68 75
TRUE	DP_INT_ML_N<3>	68 75
TRUE	DP_INT_ML_P<0>	68 75
TRUE	DP_INT_ML_P<1>	68 75
TRUE	DP_INT_ML_P<2>	68 75
TRUE	DP_INT_ML_P<3>	68 75
TRUE	LCD_IRQ_L	68
TRUE	LCD_HPD_CONN	68
TRUE	LCD_BKLT_PWM_R	63 68
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72 81
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72 81
TRUE	I2C_BKLT_SDA	63 68 71
TRUE	I2C_BKLT_SCL	63 68 71
TRUE	PP5VR3V3_SW_LCD	3X 68
TRUE	PPVOUT_S0_LCDBKLT	63 68
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 41 67
TRUE	PPVTT_S0_DDR	21 27 60 70
TRUE	PP3V3_S0	66 67 68 70 72 82 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 44 46 47 66 69 70 72
TRUE	PP3V3_S5	17 34 35 37 38 39 41 42 43 44 50 56 61 64 66 67 70 71 72
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	PP5V_S0	18 19 37 49 58 59 62 63 66 67 70 71 72
TRUE	PP5V_S3	21 37 60 66 67 70
TRUE	PP5V_S5	61 66 70
TRUE	PPBUS_G3H	30 45 56 57 63 65 70
TRUE	PPDCIN_G3H	56 57 70
TRUE	PPVCC_S0_CPU	6 8 10 46 59 70
TRUE	PPVTTDDR_S3	60 70
TRUE	PP3V3_S0SW_SSD	35 46 70
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 67 69 70
TRUE	PP1V35_S3	21 46 60 66 70

XDP

FUNC_TEST	XDP_CPU_TCK	6 18 75
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 75
TRUE	XDP_CPU_TDO	6 18 75
TRUE	XDP_CPUPCH_TRST_L	6 18 75
TRUE	XDP_CPU_TMS	6 18 75
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 75
TRUE	XDP_CPU_PRDY_L	6 18 75
TRUE	PM_RSMRST_L	12 67 77
TRUE	PM_PCH_PWROK	12 19 77
TRUE	PM_SYSRST_L	12 19 41 77
TRUE	CPU_CFG<3>	6 18 75
TRUE	PP1V05_S0	10 14 15 17 18 42 62 67 70
TRUE	GND	2X GND

Power Sequence

FUNC_TEST	SMC_ONOFF_L	39 41 42
TRUE	PM_DSW_PWRGD	12 41 77
TRUE	ALL_SYS_PWRGD	18 19 41 58 67
TRUE	PM_PCH_SYS_PWROK	12 18 19 41 77
TRUE	PLT_RESET_L	12 18 20 21
TRUE	EDP_IG_PANEL_PWR	12 68 71
TRUE	EDP_IG_BKL_ON	12 63 71

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Functional Test Points

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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NC NO_TESTs

PCH

		NO_TEST	MAKE_BASE	
NC_USB3_SPARE_D2RN	=	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	=	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	=	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	=	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	=	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	=	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	=	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	=	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	=	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	=	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	=	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	=	TRUE	TRUE	NC_USB3_EXTD_R2D_CP

NC_PCIE_ENET_D2RN	=	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	=	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	=	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	=	TRUE	TRUE	NC_PCIE_ENET_R2D_CP

NC_SATA_A_D2RN	=	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	=	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	=	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	=	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	=	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	=	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	=	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	=	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	=	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	=	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	=	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	=	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	=	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	=	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	=	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	=	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	=	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	=	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	=	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	=	TRUE	TRUE	NC_SATA_F_R2D_CP

NC_USB_EXTCN	=	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	=	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	=	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	=	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	=	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	=	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	=	TRUE	TRUE	NC_USB_6N
NC_USB_6P	=	TRUE	TRUE	NC_USB_6P
NC_USB_7N	=	TRUE	TRUE	NC_USB_7N
NC_USB_7P	=	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	=	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	=	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	=	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	=	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	=	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	=	TRUE	TRUE	NC_USB_IRP

NC_ITPXDP_CLK100MN	=	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	=	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	=	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	=	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	=	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	=	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	=	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	=	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	=	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	=	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	=	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	=	TRUE	TRUE	NC_CLINK_RESET_L
NC_LPC_CLK33M_LPCPLUS_R	=	TRUE	TRUE	NC_LPC_CLK33M_LPCPLUS_R

NC_USB_SMCP	=	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	=	TRUE	TRUE	NC_USB_SMCN

NC_SMC_INTERFACE_2	=	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

		NO_TEST	MAKE_BASE	
NC_TBT_XTAL25OUT	=	TRUE	TRUE	NC_TBT_XTAL25OUT

TP_DP_TBTSRC_ML_CP<3..0>	=	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	=	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	=	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	=	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN

NC_DP_IG_D_AUXCHN	=	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	=	TRUE	TRUE	NC_DP_IG_D_AUXCHP

NC_PCIE_CLK100M_GPUN	=	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	=	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	=	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	=	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	=	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	=	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	=	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	=	TRUE	TRUE	NC_PCIE_CLK100M_SWP

NC_PCH_GPIO64_CLKOUTFLEX0	=	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	=	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	=	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	=	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

NC_USB_4N	=	TRUE	TRUE	NC_USB_4N
NC_USB_4P	=	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	
TRUE	PCIE_TBT_R2D_N<3..0>	
TRUE	PCIE_TBT_D2R_C_P<3..0>	
TRUE	PCIE_TBT_D2R_C_N<3..0>	

TRUE	DMI_S2N_P<3..1>		
TRUE	DMI_S2N_N<3..1>		
TRUE	DMI_N2S_P<3..1>		
TRUE	DMI_N2S_N<3..1>		

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_D2R_P<1>	1	SM	BEAD-PROBE	BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	1	SM	BEAD-PROBE	BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: NC & No Test

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X425 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	*	=4X_DIELECTRIC	?
PEG3_TXRX	*	=8X_DIELECTRIC	?
PEG3_2OTHER	*	=5X_DIELECTRIC	?
PEG3_2CLK	*	=8X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG3_TXRX	TOP,BOTTOM	=12X_DIELECTRIC	?
PEG3_2OTHER	TOP,BOTTOM	=8X_DIELECTRIC	?
PEG3_2CLK	TOP,BOTTOM	=12X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG3_*	=SAME	*	PEG3_2SAME
PEG3_R2D	PEG3_D2R	*	PEG3_TXRX
PEG3_*	*	*	PEG3_2OTHER
PEG3_*	CLK_*	*	PEG3_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0> 5 12 73
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0> 5 12 73
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0> 5 12 73
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0> 5 12 73
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT 5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC 5 12
T125 DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P 6 11
T126 DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N 6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N 6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P 6 11
T151 CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N 6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P 6 11
T137 CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP 5
T138 CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP 5
T139 CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0> 6 18 72
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP 11 73
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN 11 73
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI 6 18 72
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO 6 18 72
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS 6 18 72
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK 6 18 72
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L 6 18 72
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0> 6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4> 6 18
T154 XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L 6 18 19
T155 XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L 6 18 72
T156 XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L 6 18 72
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L 6 41
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI 6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L 6 41 42 58
T158 CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD 6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTL	PM_THRMTRIP_L 6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD 6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC 6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0> 6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT 8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK 8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L 8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 9 58
T146 CPU_MEM_VREF		MEM_12MTL	CPU_DIMMA_VREFDQ 7 22
T147 CPU_MEM_VREF		MEM_12MTL	CPU_DIMMB_VREFDQ 7 22
T240 CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 71 78
T240 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B 22 25 26 71
T240 CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA 22 23 24 25 26 71 75 78
T240 CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA 22 23 24 25 26 71 75 78
T229 PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_P<3..0> 5 35 71
T231 PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_N<3..0> 5 35 71
T230 PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_P<3..0> 5 35 71
T240 PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_N<3..0> 5 35 71
T240	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_P<3..0> 35
T247	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_N<3..0> 35
T156 PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0> 5 28 71
T157 PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0> 5 28 71
T158	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0> 28 73
T159	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0> 28 73
T160 PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0> 28 73
T161 PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0> 28 73
T167	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0> 5 28 71
T168	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0> 5 28 71

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
T243 DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0> 5 68 71
T244 DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0> 5 68 71
T166	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0> 68 72 75
T167	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0> 68 72 75
T231	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0> 68
T232	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0> 68
T234	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0> 68 72 75
T233	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0> 68 72 75
T246 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P 5 68 71
T245 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N 5 68 71
T177 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P 68 72
T176 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N 68 72

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
T211 HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0> 69 71 72
T210 HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0> 69 71 72
T213 HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P 5 69 71 72
T212 HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N 5 69 71 72
T235 DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0> 5 28 71
T236 DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0> 5 28 71
T237	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0> 28
T238	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0> 28
T239 DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0> 5 28 71
T240 DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0> 5 28 71
T241	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0> 28
T242	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0> 28
T222 TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P 28
T224 TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N 28
T221	DP_85D		DP_TBTSNK0_AUXCH_C_P 12 28 71
T220	DP_85D		DP_TBTSNK0_AUXCH_C_N 12 28 71
T227 TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P 28
T226 TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N 28
T223	DP_85D		DP_TBTSNK1_AUXCH_C_P 12 28 71
T228	DP_85D		DP_TBTSNK1_AUXCH_C_N 12 28 71

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 73
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 73
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 73
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 73
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 73
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 73
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 73
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 73
T213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_85D	USB	USB_EXTA_P	13 38
	USB_85D	USB	USB_EXTA_N	13 38
T24	USB_85D	USB	USB_EXTA_MUXED_P	38
T24	USB_85D	USB	USB_EXTA_MUXED_N	38
T23	USB_85D	USB	USB_LT1_P	38
T23	USB_85D	USB	USB_LT1_N	38
	USB_85D	USB	NC_USB_EXTCP	13 73
	USB_85D	USB	NC_USB_EXTCN	13 73
T23	USB_85D	USB	NC_USB_SDP	13 73
T23	USB_85D	USB	NC_USB_SDN	13 73
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_85D	USB	NC_USB_SMCP	73
	USB_85D	USB	NC_USB_SMCN	73
T28	USB_85D	USB	NC_USB_6P	13 73
T28	USB_85D	USB	NC_USB_6N	13 73
T28	USB_85D	USB	NC_USB_7P	13 73
T28	USB_85D	USB	NC_USB_7N	13 73
	USB_85D	USB	USB_EXTB_P	13 69 72
	USB_85D	USB	USB_EXTB_N	13 69 72
T26	USB_85D	USB	NC_USB_EXTDP	13 73
T25	USB_85D	USB	NC_USB_EXTDN	13 73
	USB_85D	USB	USB_BT_P	13 34
	USB_85D	USB	USB_BT_N	13 34
	USB_85D	USB	USB_BT_CONN_P	34 72
	USB_85D	USB	USB_BT_CONN_N	34 72
T28	USB_85D	USB	NC_USB_IRP	13 73
T28	USB_85D	USB	NC_USB_IRN	13 73
T28	USB_85D	USB	USB_TPAD_P	13 39 72
T28	USB_85D	USB	USB_TPAD_N	13 39 72
T30	USB_85D	USB	USB_TPAD_R_P	
T30	USB_85D	USB	USB_TPAD_R_N	
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T22 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
T23 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T23 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
T22 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 69 72
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 69 72
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	69 72
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	69 72
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 69
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 69
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 73
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 73
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 73
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 73
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 73
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 73
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 73
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 73

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T256 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T255 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
T253 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?
SPI3X	*	=3x_DIELECTRIC	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 44 69 71 72
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 44 69 71 72
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
	HDA_45S	HDA	HDA_SDOUT_R	11 19
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 69 72
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 69 72
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 69 72
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 69 72
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 72
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 72
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
[1304]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
[1305]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
[1276]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 72
[1276]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 72
[1275] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
[1274] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
[1277]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
[1278]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
[1270] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
[1269] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
[1271]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
[1272]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
[1263]	CLK_LPC_45S	CLK_LPC	NC_LPC_CLK33M_LPCPLUS_R	11 73
[1249] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
[1250] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
[1248] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
[1253] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
[1254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
[1257] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
[1258] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
[1255] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
[1256] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
[1259] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
[1260] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
[1265]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 72
[1266]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 72
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
[1274]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
[1273]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
[1267] PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
[1268]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
[1313] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
[1314] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
[1315] PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
[1316] PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
[1320] PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 67 72
[1321] PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 72
[1322] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 72 77
[1323] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 72 77
[1324] PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 72
[1319] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 72
[1318] PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
[1317] PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
[1326] PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 72
[1325] PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
[1310] SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CLK	50 72
[1305] SPI_MLB	SPI_45S	SPI	SPI_CLK	50
[1306] SPI_MLB	SPI_45S	SPI	SPI_CLK_R	13 50
[1308] SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CLK	50
[1309] SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CLK	41 50
[1303] SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CS_L	50 72
[1304] SPI_MLB	SPI_45S	SPI	SPI_CS0_L	50
[1307] SPI_MLB	SPI_45S	SPI	SPI_CS0_R_L	13 50
[1302] SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CS_L	50
[1301] SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CS_L	41 50
[1300] SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO1_MISO	50 72
[1305] SPI_MLB	SPI_45S	SPI	SPI_MISO	13 50
[1306] SPI_MLB	SPI_45S	SPI	SPI_MISO_R	50
[1307] SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO1_MISO	50
[1311] SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MISO	41 50
[1306] SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO0_MOSI	50 72
[1305] SPI_MLB	SPI_45S	SPI	SPI_MOSI	50
[1305] SPI_MLB	SPI_45S	SPI	SPI_MOSI_R	13 50
[1377] SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO0_MOSI	50
[1376] SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MOSI	41 50
[1375] SPI_MLB_IO2	SPI_45S	SPI3X	SPI_IO<2>	13 50
[1374] SPI_MLB_IO2	SPI_45S	SPI3X	SPI_MLB_IO2_WP_L	50
[1374] SPI_MLB_IO2	SPI_45S	SPI3X	SPI_ALT_IO2_WP_L	50 72
[1378] SPI_MLB_IO3	SPI_45S	SPI3X	SPI_IO<3>	13 50
[1372] SPI_MLB_IO3	SPI_45S	SPI3X	SPI_MLB_IO3_HOLD_L	50
[1370] SPI_MLB_IO3	SPI_45S	SPI3X	SPI_ALT_IO3_HOLD_L	50
[1345] SPI_TPAD	SPI_45S	SPI	TPAD_SPI_SCLK	39 71 72
[1346] SPI_TPAD_CS	SPI_45S	SPI	TPAD_SPI_CS_L	39 71 72
[1347] SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MISO	39 71 72
[1345] SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MOSI	39 71 72

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: PCH Constraints 2

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 71 75
		MEM_PWR	PP0V75_S3_MEM_VREFCA 22 23 24 25 26 71 75
		MEM_PWR	PP1V35_S3_MEM 22 23 24 25 26 46 70

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 73
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 73
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE
161	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L
162		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT
163	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L
164	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>
165	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>
166	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>
167	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>
168	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>
169	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>
170	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>
172	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P
173	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N
174		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P
175		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N
176	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P
177	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N
178		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P
179		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N
180			S2_MEM_PWR	PP1V35_CAM
181			S2_MEM_PWR	PP0V675_CAM_VREF
182			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA
183			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 72
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 72
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	41 44 56 57 72
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 72
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

X425 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47 66
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47 66
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	47 68 82
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	47 68 82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	47 68 82
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	47 68 82
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PCH_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PCH_N	
	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
			DIFFERENTIAL_PAIR	
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1 CPUVR_ISNS1_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1 CPUVR_ISNS1_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2 CPUVR_ISNS2_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2 CPUVR_ISNS2_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3 CPUVR_ISNS3_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3 CPUVR_ISNS3_N	46 59
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	82
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	46 62
	THERM_1TO1_45S	THERM	P1V05S0_CS_N	46 62
			DIFFERENTIAL_PAIR	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_P	62
	THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMDP	28 48
	THERM_1TO1_45S	THERM	TBT_THERMDN	48
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

X425 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
	AUDIODIFF	AUDIO	RSUBIN_P	53
	AUDIODIFF	AUDIO	RSUBIN_N	53
	AUDIODIFF	AUDIO	LSUBIN_P	53
	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
	DIFFPAIR	AUDIO	HS_MIC_P	51 54
	DIFFPAIR	AUDIO	HS_MIC_N	51 54
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53

SB_POWER	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 66 67 70 71 72
SB_POWER	PP3V3_S0	60 67 68 11 12 13 14 15 17 19 29 30 33 35 44 45 46 47 48 49 51 52 55
SB_POWER	PP1V35_S3RS0_CPUDDR	70 72 8 10 21 66 67 70
GND	GND	

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